60475580

CONTROL DATA

CORPORATION

AUTO RESTART LOADER

QSE 20030

GENERAL DESCRIPTION
OPERATION AND PROGRAMMING
INSTALLATION AND CHECKOUT
THEORY OF OPERATION
DIAGRAMS
MAINTENANCE
PARTS DATA

HARDWARE MAINTENANCE/REFERENCE MANUAL

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1.1 GENERAL

This manual describes FV679 CYBER 18 Auto Restart Loader, FV498-A Stall Alarm Panel, and DN134-A IOM Adapter.

The FV679 Auto Restart Loader (ARL) consists of a PWA and a paddle board which occupy one A@ card slot in the CYBER 18 processor. It performs multiple functions:

- Loads data stored in the programmable read only memory (PROM) on the Restart Loader board into the processor when activated manually or by "power on" or external signals.
- Generates alarm and interrupt if the processor fails to update any of two interval timers.
- Provides two 16-bit programmable digital I/O channels that can be used for input or output to external devices.
- Interfaces with 1500 series IOM peripherals in conjuction with the DN134-A IOM Adapter.

The FV498-A Stall Alarm Panel is connected to the FV679 ARL by the XA124-A Stall Alarm Panel cable. The panel contains stall alarm display, audible alarm, two relays and switches.

The DN134-A IOM Adapter occupies one slot on a 1750-2 Computer Interface Expander (CIE) and interfaces with up to seven CIE's.

1.2 AUTO RESTART LOADER (ARL)

The Auto Restart Loader (ARL) consists of one standard MP size multi-layer board and one 2" x 12 1/2" two-layer paddle board.

The ARL board assembly, containing TTL compatible CMOS LSI chips for control logic and TTL bipolar SSI/LSI chips for the rest of the logic, interfaces with FV498-A stall alarm panel, DN134-A IOM adapter, and external digital input or output devices via a paddle board.

The paddle board mounted on the processor backplane provides connections to the above devices. It also allows interrupt signals and other control signals to be jumper-wired to the processor.

Control of the ARL is done by the Z80A microprocessor and controlware stored in a PROM (1k x 8-bit words). The ARL provides two 24-pin sockets where customer-furnished PROM(s) can be mounted for restart loading functions.

1.2.1

The ARL detects DC power (+5V, +12V, -12V) when power is turned on and clears the POWERFAIL signal. In the meantime, it monitors ACFAIL signal from the main power supply in the processor, and sets the POWERFAIL signal when failure occurs. The signal can be jumper-wired on the processor backplane so as to trigger power failure handling hardware in the processor. Being cleared, it also activates

1.2.1 {Continued}
restart loading sequence when the on-board jumper is installed.

1.2.2 The ARL transfers contents of user-furnished PROM into the CPU through the serial Deadstart path, when activated. Transfer rate is determined by setting UART clock speed select switch on the I/O TTY board. PROM size varies from 512x8-bit words up to 4Kx8-bit words.

1.2.3 The ARL performs similar functions as the FV4A3 Stall Alarm unit does. It sets stall alarm in the following conditions:

- An overflow of any of two timers, when not periodically reset or preset by the computer program.
- A contact closure input from an external equipment {field stall}.
- A function command issued by the computer {computer stall}.

When one of the above conditions is met, the ARL lights LED display at the bottom front corner of the board and turns on four current drivers which set a stall alarm light, an audible alarm, and two contact relays on the FV498-A Stall Alarm Panel.

1.2.3 {Continued}

Stall Alarm features are:

- The audible alarm can be shut off by the Stall Alarm Panel Reset Switch
- Two Stall counter timers can be shut off by setting the Stall Alarm Panel Mode Select Switch in "OFF" position.
- Stall interrupt to the computer can be enabled/disabled by a function command.
- Stall conditions can be cleared by a function command or by a Master Clear in the computer.

1.2.4 The ARL transfers two 16-bit digital data between the computer and digital I/O devices. The 16-bit word can be divided into two 8-bit bytes, of which operation modes can be independently selectable by a function command. The Selectable modes are:

- Word Mode/Byte Mode - Transferred data contains 16-bit valid data in word mode, and 8-bit valid data in byte mode.
- Test Mode - Overrides byte mode and I/O mode to be in special word mode which allows both input mode and output mode, to test the data channel{s}.
- Inversion/non-inversion - Matches data signal polarity of external digital equipment{s}.
- Async/sync mode - Data transfer is controlled by the computer in Async mode, and by external device{s} in Sync mode. {Refer to Section Four, Theory of Operation}

1.2.4 (Continued)

- Input mode/output mode - Input mode for input device with which the ARL interfaces, and vice versa.

Once the modes of operation are selected, the ARL operates in a similar manner as in the DA101/401 Digital Input Unit (DIU) and/or in the DA502 Digital Output Unit (DOU).

1.2.5 The ARL provides AQ channel to the DN134-A IOM Adapter which interfaces with the 1750-2 CIE. It buffers eight interrupt signals from the Adapter to the computer, and sends out AQTEST signal which is set or cleared by a function command and which puts the Adapter on test mode. (Refer to Section 1.4 for the AQ test mode).

Addressing of the IOM Adapter is completely independent from that of the ARL.

1.3 STALL ALARM PANEL (SAP)

The ARL interfaces with the FV498-A Stall Alarm Panel (SAP) which is used with the 1500 series FV4A3 Stall Alarm Unit, via the XA241-A Stall Alarm Panel Cable (Refer to CDC - Pub 88981000).

The SAP has a removable mounting plate that will provide for either 19-inch rack mount or desk-top mount. It operates in the following manner:

- Power and Ground - provided by the ARL through the SAP cable. +5V, 40mA
- LED display, audible alarm, and two contact relays are driven by the ARL.
- Manual Reset switch - pushbutton switch shuts off the audible alarm. The alarm will be back on only after stall conditions are cleared.
- Operating Mode Select switch - disables counter timer clock in the ARL when it is in "OFF" position and enables the clock when it is in "COMPUTER" or in "MANUAL" position.
- Test switch - has three positions: ON/OFF/TEST for enabling/disabling/testing the audible alarm.
- Relays - Two mercury-wetted Form C relays are activated in response to an alarm condition and are intended for use in controlling external equipment operation(s). Contact rating is 250 VA or 500 VDC at 5 amps.
- Field Stall Inputs - Two pairs of field stall inputs (one signal input and one ground) can be of either TTL logic level or contact closure type.

The XA241-A SAP cable connects the SAP at the distance of up to 25 feet from the ARL.

1.4 DN1134-A IOM ADAPTER

The DN1134-A IOM Adapter contains TTL SSI chips mounted on a half size of a standard IOM card. It occupies card position one of a 1750-2 CIE and is connected with the ARL by a pair of cables. Length of the cable is limited to 20 feet.

The adapter includes input/output signal buffers, output data register, equipment code comparator, module decoder, and timing circuits in order to convert the 1750-2 CIE to a TTL version Computer Interface Unit (CIU) in the analogy with the 1750-1 CIU.

Timing circuits adjust read/write signal timing to comply with the 1700 computer AQ conventions, and send REPLY signal to the ARL (eventually to the computer) during the AQ Test Mode operation.

A function command to the ARL sets/clears the AQ Test Mode, in which data bus to the CIE's can be tested by a diagnostic program.

2.1 OPERATION

2.1.1 Auto Restart Loader

The operations that the Auto Restart Loader perform are described in the following paragraphs.

2.1.1.1 Adjustments

The DC voltage detection circuits on the ARL require adjustments as follows:

1. +5V Adjustment: Lower the 5V power supply to low margin (+4.75V) and, watching logic level of Test Point at the front edge of the ARL, turn the +5V trimmer (R18) counter-clockwise. As soon as the test point logic level changes to logic 0 (+0.8V or less), turn the trimmer clockwise slowly until the test point logic level changes back to logic 1 (+2.5 V or higher).

2. +12V Adjustment: Lower the +12V power supply to low margin (+11.4V) and repeat the above steps with the +12V trimmer (R16).

3. -12V Adjustment: Increase the -12V power supply to upper margin (-11.4V) and repeat the above steps with the -12V trimmer (R12).

2.1.1.2 Restart Loading

The Auto Restart Loader, when activated by one of the methods described below, checks the checksum of the PROM contents, and loads data stored in the Programmable Read Only Memory (PROM) into the processor in the Serial Deadstart Mode. It starts loading the PROM data at location $000 until control code is read from the PROM and directs otherwise. Refer to 2.2 Programming Information for the control code description. Checksum error will turn on error display LED at the upper front corner of the board.

Methods of Activating the Loading Function

1. Power-On - When the power-on jumper is installed on the board, the restart loading operation starts at the power on time.
2. Manual Switch - A momentary manual switch mounted on the front edge of the board starts the operations when pressed.
3. External TTL signal - An external TTL signal activates loading at its negative going transition time. A backplane jumper wire should be connected to J3-10 from customer equipment, (refer to Table 3.6) and on-board jumper wire should be installed per Table 3.3. The Deadstart Mode (SM204/) signal can replace this signal if on-board jumper wire is so installed per Table 3.3.

2.1.1.2 (Continued)

4. External Contact Closure Output - An externally provided contact closure signal can activate the loading operation at its negative going transition time.
5. AQ Function Command - AQ Function command can activate the loading operation. Unlike the above methods, the command indicates the ARL starting location - contents of A register or address set by a PROM address switch. Refer to Paragraph 2.2 Programming Information.

PROM Size

The ARL provides two IC sockets (A4 and A5) to mount pre-programmed PROMs furnished by user. Refer to Table 3-4.

PROM Contents

Contents of the PROMs are grouped in three as follows:

- ASCII code - is read from the PROM and transferred to the processor.
- Control code - most significant bit of the PROM data is set to "1" to be distinguished from ASCII data. See 2.2 Programming Information for definitions of the codes.
- Binary Data - preceded by a control code. Upper 4-bit and lower 4-bit data are converted to ASCII before being transferred.

1.1.2 (Continued)

PROM Address Switch

The PROM Address Switch is a set of eight rocker switches in a Dual-in-Line Package (DIP) at Location G3, and selects the PROM address from which loading operation can take place. Actually, the switch specifies 16-word block number to address 4K word with eight bit switch. Refer to 2.2 Programming Information for additional information.

Serial Data Transfer

Data is seven bits in length, preceded by a start bit and followed by an even parity bit and two stop bits.

Transfer rate is set by the baud rate select switch on the I/O-TTY board. Available rates are 110, 300, 1200 and 9600 baud.

The data transferred into the CPU may do the following:

1. Master clear the CPU
2. Set up all registers in the CPU with an initial data.
3. Set/clear mode select switches - step enable, selective stop, selective skip, and Protect Switch.
4. Clear/store main memory or micro memory
5. Set/Reset the Program Protect bits in the Main Memory
6. Generate a "GO" signal to execute the program in the "RUN" mode and stop the CPU.

1.1.2 (Continued)

7. Set up the breakpoint register if the panel interface board is installed.

8. Set up the program counter at an initial location of a program.

Restrictions

1. The character "?" is used as the Master Clear in the CYBER 18 processor. The character following the "?" is transferred after the Master Clear is completed.

2. The suppress console transmit bit on the Function Control Register (FCR) shall be set to suppress console transmit (J48) to avoid pseudo half duplex operation. It should be cleared at the end of loading (J40).

3. When the processor is running in Macro mode, registers used in that mode shall not be altered by the loaded data. Example: In CYBER 18, file F2 shall not be cleared, since 1700 Emulator uses the file.

4. When both power on restart from the ARL and auto restart by the processor are enabled, (power-up restart jumper is installed on the ARL and AR-ENABLED at N96 on the processor backplane is set high), program run away may occur. First character sent from the ARL must be ? (Master clear) to avoid this condition.

5. At the beginning of loading or after transferring ? (Master Clear), ESC (escape key, or ASCII $1B) should follow to set console in panel mode. At the completion of loading, @ (ASCII $40) should follow to set console in program mode.

2.1.1.3 Stall Alarm

- Stall time delay can be set by a function command (Refer to Paragraph 2.2 Programming Information) within ranges as follows:
  Counter No. 1 - 1 msec to 256 msec with 1 msec increment.
  Counter No. 2 - 100msec to 25.6 sec with 100msec increment.

- Stall counter clock is enabled/disabled by the mode select switch on the stall alarm panel, or by STLOFF/ signal at J7-1 when stall alarm panel cable is not connected to the ARL. When the clock is enabled, stall function command and stall data command control the counters.

- When the stall alarm panel cable is not connected to the ARL, negative going contact-closure/TTL signal (FLDSTL/) at J7-3 sets field stall.

2.1.1.4 Digital Input/Output

- Operation modes of digital data transfer are controlled by a function command in 2.2 Programming Information.

- Control signals (REQUEST, RESET, RESPONSE) may not be used in Async mode. In word mode operation, control signals at the least significant byte shall not be used.

- Install cables per Table 3-8. Connector to the ARL end shall be 2x7 0.100 inch spacing.

2.1.1.5 IOM Interface

- Equipment code of the IOM can be same as that of the ARL when its module number is other than zero.
- AQTEST/ signal can be set/cleared by a function command to the ARL, and can set the IOM adapter in Test mode.
- STALL/ signal is sent to the IOM and allows 1500 series IOM devices to respond to a stall condition.

2.1.2 Stall Alarm Panel

The stall alarm panel (SAP) contains the following features:

- An indicator light will be turned on when a stall condition is set. Once set, it can only be reset by a stall function command or a master clear.
- An audible alarm can be shut off by a "RESET" switch, a stall function command or a master clear.
- A three position switch that (1) activates the audible alarm whenever a stall condition is set (ON), (2) disables the audible alarm (OFF), or (3) provides a continuous tone (TEST).
- A manual RESET button that, when pressed, resets the audible alarm.
- A mode select switch that disables stall timer counter clock (OFF) or enables it (MANUAL or COMPUTER).

TABLE 2-1. STATION NUMBERS

STATION NUMBER	WRITE OPERATION	READ OPERATION
0	Unit Function	Unit Status
1	Digital I/O Function	NOT USED
2	Stall Data	NOT USED
3	Stall Function	Stall Status
4	Digital Data Out Byte 0	Digital Data In Byte 0
5	Digital Data Out Byte 1 or Word 0	Digital Data In Byte 1 or Word 0
6	Digital Data Out Byte 2	Digital Data In Byte 2
7	Digital Data Out Byte 3 or Word 1	Digital Data In Byte 3 or Word 1
8	Restart Loader Function	NOT USED
9	ARL Memory Address	ARL Memory Contents
10 - 15	NOT USED	NOT USED

2.1.2 (Continued)

- A terminal block that provides two contact C relay output terminals and two pair of field stall terminals (field stall signal/ground pair). (Refer to Table 3-7).

2.1.3 IOM Adapter

- A jumper is provided to respond to equipment code number 0 through F. The adapter requires two successive numbers and the jumper provides this selection (e.g. 2 and 3, 8 and 9, C and D, etc.)

- A jumper is to be installed to allow only protected A/Q commands to be acknowledged.

- Module select jumper and interrupt jumper connections are described in CIU/CIE manual (88980100 Sec. 2.2.3 and 2.2.4).

2.2 PROGRAMMING INFORMATION

2.2.1 Auto Restart Loader

ARL acknowledges an A/Q command that meets the following requirements:

- W Field (most significant five bits of Q register) is equal to zero.

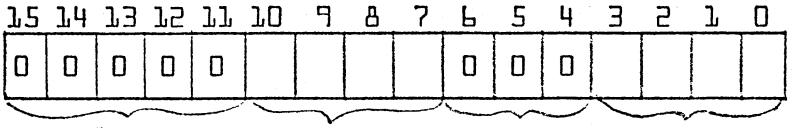
- 4-bit equipment code matches with the equipment select switch setting.

- 3-bit module number is equal to zero. (same as selecting CIU in the 1500 series IOM)

2.2.1 (Continued)

- 4-bit station numbers shall be one of those shown in Table 2-1.

The Q-register description is as follows:



W=Field W=0 | Equipment Code (1 of 16) | Module =0 | Station Number (1 of 16)

The A/Q commands allowed in the ARL are described as follows:

The Unit Function

When the Q register contains the proper code to select station number 0, the contents of the A register during the output instruction performs the unit function command as defined below.

A register

Bit 0=1: Clear digital output data on Stall condition

Bit 1: Not used

Bit 2=1: Enable interrupt, =0: clear interrupt

Bit 3=1: AQ test

Bit 4 - Bit 7: Not used

Bit 8=1: Invert Request 0 polarity, since it is active low.

2.2.1 {Continued}

Bit 9=1: Invert Request 1 polarity, since it is active low.

Bit 10=1: Invert Request 2 polarity, since it is active low.

Bit 11=1: Invert Request 3 polarity, since it is active low.

Bit 12=1: Invert Response 0 polarity to get active low signal.

Bit 13=1: Invert Response 1 polarity to get active low signal.

Bit 14=1: Invert Response 2 polarity to get active low signal.

Bit 15=1: Invert Response 3 polarity to get active low signal.

The Unit Status

When the Q register contains the same code as in the unit function command, the input operation to the CPU will obtain the status of the unit as defined below:

A register

Bit 0=1: Not Used

Bit 2=1: Digital I/O ready. The Digital I/O function command clears this bit until the I/O modes are fully set up. The digital data transfer command will be rejected without this bit set.

Bit 3=1: Stall condition is set. When interrupt is enabled, stall interrupt is also set.

2.2.1 {Continued}

Bit 4=1: Digital Data Transfer Request 0 set {Byte 0}

Bit 5=1: Digital Data Transfer Request 1 set {Byte 1}

Bit 6=1: Digital Data Transfer Request 2 set {Byte 2}

Bit 7=1: Digital Data Transfer Request 3 set {Byte 3}

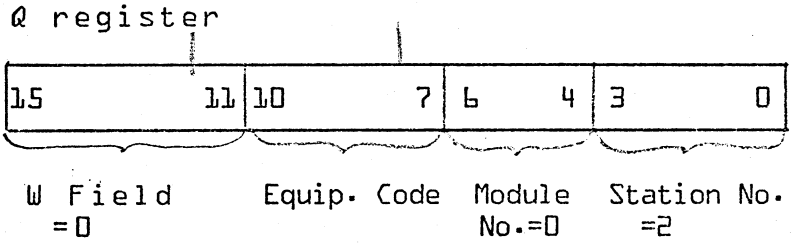
Bit 8 - Bit 15: NOT USED

The following commands control the stall alarm operations:

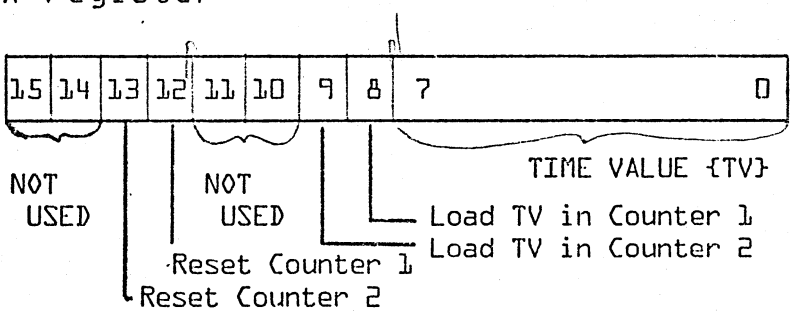
Stall Data Command

The counter can be set or reloaded to a preset time value by an "OUTPUT FROM A" instruction with the following Q and A register contents to avoid counter overflow interrupt.

Q register



A register

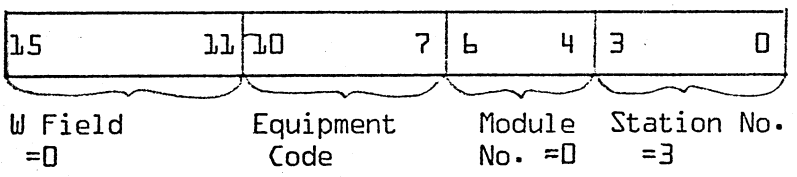


2.2.1 {Continued}

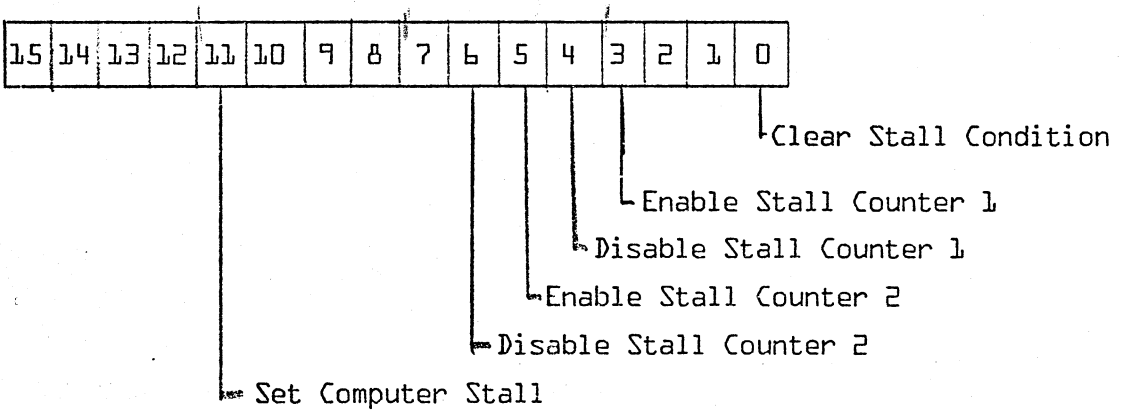
Stall Alarm Function Command

The Stall Alarm operation is controlled by a Stall Function command with the following information in the Q and A registers when the computer executes "OUTPUT FROM A" instruction.

Q register



A register



A0=1: Clears all the Stall conditions and disables the stall interrupt.

A3=1: Enables the stall counter 1 and the overflow interrupt.

A4=1: Disables the stall counter 1 and the overflow interrupt.

2.2.1 {Continued}

A5=1: Enables the stall counter 2 and the overflow interrupt.

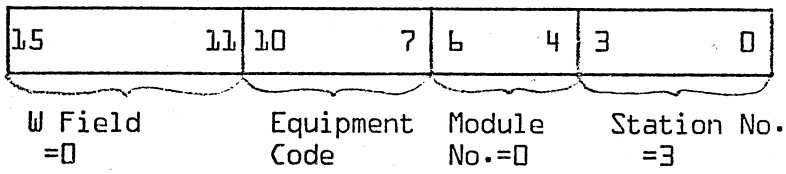
A6=1: Disables the stall counter 2 and the overflow interrupt.

A11=1: Sets the computer stall condition.

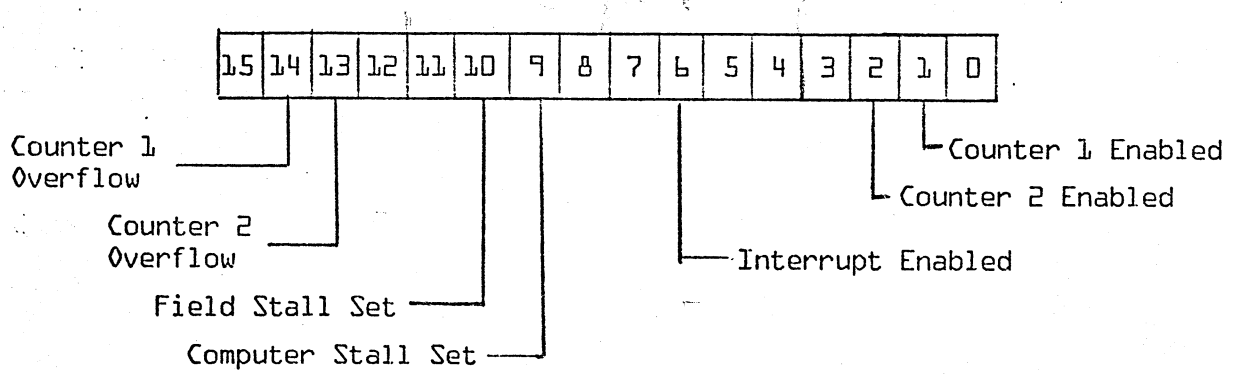
The other bits are not used.

Stall Status Command

The Stall Status can be obtained by doing an input command with the following in the Q register.



Status will be input into the A register as follows:

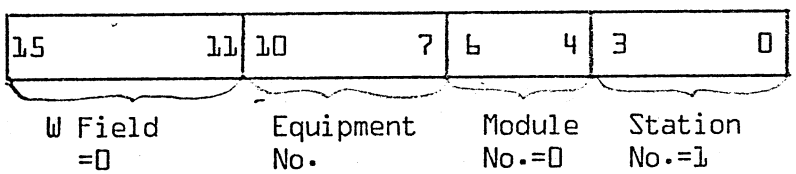


2.2.1 {Continued}

The Digital I/O Functions

The operation modes are selected by the AQ output commands with the following information in the Q and A registers.

Q register



A register

A0=1: Byte 0 in the input mode

A1=1: Byte 1 in the input mode

A2=1: Byte 2 in the input mode

A3=1: Byte 3 in the input mode

A4=1: Byte 0 in the Async mode

A5=1: Byte 1 in the Async mode

A6=1: Byte 2 in the Async mode

A7=1: Byte 3 in the Async mode

A8=1: Byte 0 inverted

A9=1: Byte 1 inverted

A10=1: Byte 2 inverted

A11=1: Byte 3 inverted

A12=1: Byte 0 and Byte 1 in the word mode {word 0}

2.1 (Continued)

A13=1: Byte 0 and Byte 1 in the test mode

A14=1: Byte 2 and Byte 3 in the word mode (word 1)

A15=1: Byte 2 and Byte 3 in the test mode

1. Byte Mode - Each 8-bit data byte can be transferred in its own modes and the rest of the A register is ignored.
2. Word mode - Two bytes of data are in the same operation modes and are transferred together. Unused control signals and the station numbers are ignored.
3. Synchronous mode - In the synchronous mode, data transfer is controlled by the external I/O device. In the input mode, the external device places the data to the unit and sends a REQUEST. The unit recognizes the REQUEST and sets the interrupt to the computer. The computer in turn initiates an AQ read cycle upon receipt of the interrupt. The unit responds to the read when the equipment code, the module number, and the station number are correct, by transferring data from the device to the computer and by sending a REPLY. When the data transfer to the computer is completed, the response signal is sent to the device until the request is dropped. The interrupt is cleared by the AQ read operation.

2.2.1 {Continued}

3. {Continued}

In the output mode, the external unit sends REQUEST. The unit recognizes the request and sets the interrupt to the computer. The computer initiates an AQ write operation upon receipt of the interrupt. The unit responds to the write command {when the equipment code, the module number, and the station number are correct} by transferring data from the computer to the device via an output buffer register on the board and by sending a reply. The unit sends a response to the device until the request is dropped. The interrupt is cleared by the AQ write operation.

4. Asynchronous Mode - In the Asynchronous mode, data transfer is controlled by the computer. In the input mode, the computer performs a read operation via the unit from the external device when the equipment code, the module number, and the station number are correct. The unit sends a reply to the computer and a response to the external device, respectively.

In the output mode, the computer outputs data via the unit to the external device with the correct equipment code, the module number, and the station number. The unit sends a reply to the computer and a response to the external device.

2.2.1 {Continued}

4. {continued}

In the Asynchronous mode, the device may or may not send a request to set an interrupt. However, the unit always responds to the computer with a reply regardless of the interrupt status, whereas in the synchronous mode, uninterrupted data transfer operation from the computer is rejected.

5. Polarity inversion - Each group of 8-bit data polarity can be selected by the I/O Function commands and the polarity of the control signals by the unit function commands.

6. Test Mode - When selected, the test mode sets the operation modes in the Asynchronous word mode regardless of the I/O Function commands. However, the data polarity will follow as defined by the commands. The following procedure is recommended.

Test Procedure

1. Select the test mode by the Digital I/O Function command.
2. Load the Q register with a destination address and the A register with a known test data.
3. Output the data from the A register.
4. Alter the contents of the A register.
5. Input the data to the A register.
6. Compare the contents of the A register with the expected data.

2.2.1 {Continued}

6. {Continued}

7. Repeat the above steps for another Word.

8. Change the polarity selection and repeat the above steps to check the polarity selection hardware.

Note that the test mode is NOT allowed to be used when a cable assembly is installed between the unit and an external input device.

7. Input Mode - When the input mode is selected, the data from the external device is transferred to the CPU during the read operation. In the byte mode, the specified byte contains valid data from the device and the other 8 bits may not be usable.

An attempt to write data in this mode is internally rejected {the unit does not respond}.

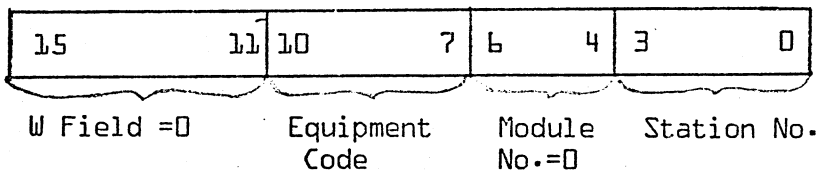
8. Output Mode - In the output mode, the data from the computer is transferred to the external device via the data buffer register on the board. The data to the device will be retained by the register until the next data is transferred. In the byte mode, the specified 8-bit data only is transferred.

2.2.1 {Continued}

The Data Transfer

Once the operation modes are selected, each byte or each word can be transferred with the following information in the Q register and with the data of the specified byte{s} in the A register.

Q register



1. Word Mode

   Word 0 - Station number is five. All 16-bit data in the A register are transferred.

   Word 1 - Station number is seven. All 16-bit data in the A register are transferred.

2. Byte Mode

   Byte 0 - Station number is four. The least significant 8-bit data in the A register are transferred.

   Byte 1 - Station number is five {the same station number as the Word 0}. The most significant 8-bit data in the A register are transferred.

   Byte 2 - Station number is six. The least significant 8-bit data in the A register are transferred.

2.2.1 {Continued}

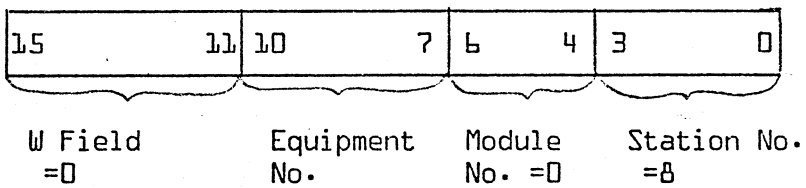
Byte 3 - Station number is seven {the same station number as the Word 1}. The most significant 8-bit data in the A register are transferred.

The AQ Restart Operations

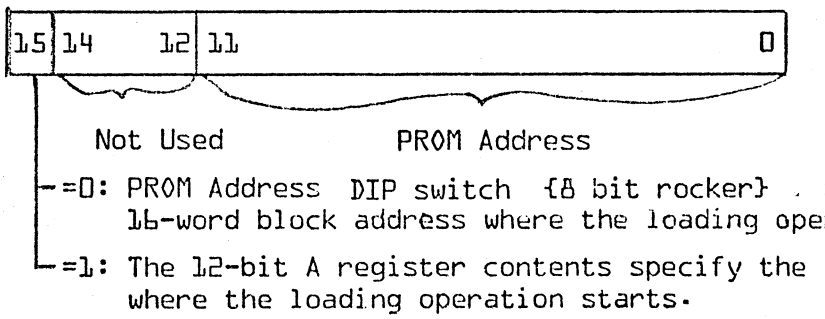
The Deadstart Loading operation can be initiated by an AQ command. The loading operation starts from a PROM location specified either by the contents of the "A" register or by the PROM address DIP switch, instead of starting from the location "zero" as in the normal operation described in preceding paragraphs.

The Deadstart command is issued by outputting the following information in the Q and A registers.

Q register



A register



ARL Memory Read/Write

When the Q register contains the proper code to select station number 9, the contents of the A register during the output instruction specify memory address of the ARL, of which contents can be read during the input instruction. The A register will contain upper eight bit bytes of data from address specified by the output instruction and lower byte of data from the address +1.

The ARL memory is mapped as shown in Table 2-2.

TABLE 2-2

ADDRESS RANGE	DESCRIPTION
$0000 - $03FF	ROM - Control ware
$1000 - $1003	8255 DIO Ports
$2100 - $21FF	RAM - Scratch patch/stack point
$8000 = $8FFF	PROM - User Program

Restart Control Codes

During restart operations, the ARL checks sign bit {most significant bit} of the user PROM contents. When the bit is not set, the data is assumed as an ASCII data and is transferred to the processor. When the bit is set, the data is interpreted as a control code. The code does the control functions as described below.

2.2.1 {Continued}

1. $BC - This control code forces the unit to replace the current PROM address counter with the word block address set by 8-bit DIP switch and continue loading from the selected program. The new location shall contain ASCII data or control code but not binary data.

2. $BB - This control code halts the loading operation

3. $8XYZ - This control code is in two 8-bit format to specify the number of times {$XYZ+1} the zero and the terminator {0:} shall be transmitted. This code clears any memory up to 4096 locations.

4. $AXYZ - This control code is in two 8-bit format to specify the number of the PROM locations {$XYZ+1} where the binary data is stored. The code can specify up to 4096 locations.

   A terminator {:} is automatically transmitted to group the converted data into four characters. $XY8+1 shall be an even number.

5. $CXYZ - This control code is in two 8-bit format to specify the number of the PROM locations {$XYZ+1} where the binary data is stored. The code can specify up to 4096 locations. A terminator {:} is automatically transmitted to group the converted data into the eight characters. $XY8+1 shall be divisible by 4.

2.2.1 {Continued}

PROM Programming Notes

Following are the notes the user should keep in mind during PROM programming for restart loading operations.

1. Master clear {?} shall be followed by ESC.
2. Suppress console transmit shall be set during the restart loading.
3. File F2 shall not be cleared when the processor is running in macro mode.
4. PROM address to be selected by the PROM address switch should be divisible by 16.
5. At the end of restart loading, Suppress Console Transmit may be cleared.
6. At the end of restart loading, @ may be transmitted to set the console in program mode.

2.3 CONTROL SIGNALS

2.3.1 REPLY/REJECT

The ARL sends reply/reject signal to the processor within 10 usec. in response to A/@ commands. When the ARL fails to respond within 10 usec., internal reject occurs. Reject conditions of the ARL are:

External Reject Conditions

- The CPU attempts identical commands more than twice before the followup routine of the first one is completed. Exception - Digital data I/O command and unit status command do not require follow up routine.

2.3.1 {Continued}

- The AQ command is unprotected when the Program Protect mode on the loader is set.
- The CPU attempts a digital data I/O operation in the Sync mode, when the REQUEST signal from an external device is not set.
- The CPU attempts a digital data I/O command when the follow-up routine of the Digital I/O Function command is not completed yet.

NOTE: Followup routine is a routine which executes AQ command right after the command is received. When multiple AQ commands are sent to the ARL they are all stacked up sequentially and then are executed.

Internal Reject Conditions

- The Q word contains an incorrect equipment code or incorrect module number.
- The Q word contains an unused station number. {Refer to Table 2-1 Station Numbers}
- In a digital I/O operation with the station number four through seven,
  - Data output operation is attempted, when the input mode is set.
  - Data input operation is attempted, when the output mode is set.

2.3.1 (Continued)

- Byte 0 operation is attempted, when word 0 or Test 0 is set.
- Byte 2 operation is attempted, when word 1 or Test 1 is set.

Note that in the Test mode data input and output operations are both allowed.

The IOM Adapter reply/reject depends on digital devices in the IOM.

2.3.2 Interrupts

The ARL provides nine interrupts to the processor - eight from IOM devices and one from the ARL itself.

Interrupt from the ARL is inhibited by the Master Reset signal or by the Unit Function Command. It is enabled by the Unit Function Command and an I/O instruction to the ARL following the command.

When an interrupt is enabled, the following conditions set the interrupt:

- Stall counter 1 or 2 overflows
- Computer Stall is set.
- Field Stall is set.
- Digital I/O device sets REQUEST Signal.

These conditions can be found in the Unit Status Command.

2.3.2 {Continued}

Interrupts from the IOM are initially inhibited in the ARL by the Master Reset signal. However, reply signal from the IOM enables them. Interrupt conditions are defined by IOM devices. Refer to CIU/CIE manual and related device manuals.

2.3.3 Master Reset

The ARL transfers the Master Reset signal from the processor to the IOM Adapter {Refer to CIU/CIE Manual}.

The Master Reset signal in the ARL inhibits all the interrupt lines and clears registers and flip-flops on the ARL to set the unit in an initial condition. The signal will not, however, clear digital data transfer mode selections set by the digital I/O function command.

2.3.4 Program Protect

Since the ARL and the IOM adapter normally run in unprotected mode, the protect jumpers are not installed so that both protected and unprotected AQ commands can be responded. However, jumper holes are still provided to force the equipments to run in the protected mode when jumper is installed in the holes.

2.3.5 Character Input Mode

The ARL does not run in the character input mode, but devices in the IOM are allowed to run in that mode.

3.1 TOOLS AND TEST EQUIPMENT

No special test equipment is required to install the Auto Restart Loader and its associated equipment. If backplane wires (described later in this section) must be added or modified, the following special tools are required:

TOOL	PART NUMBER
Wire Unwrap Tool	12259138
Wire Wrap Tool	12263210

3.2 UNCRATING/CRATING

3.2.1 Uncrating

The auto restart loader printed wiring assembly, paddle board, IOM adapter, and stall alarm panel are shipped either installed in the applicable cabinet or packed into a heavy-duty cardboard carton. All cables are shipped packed into heavy-duty cardboard cartons. If shipped in heavy-duty cartons, the equipment is buffered from shock and impact damage by industrial filler. No special instructions are required to remove the equipment from the cartons.

3.2.2 Crating

Refer to the above uncrating instructions for crating the equipment.

3.3 INSPECTION

Inspect the auto restart loader, paddle board, adapter, stall alarm panel, and cables as follows:

1. Remove the items from the shipping carton or cabinet and check for obvious damage.
2. Check the contents of each carton against the packing list.
3. Examine all connector plugs for possible bent, missing, or broken pieces.
4. Inspect all cables for damage to the insulation and shield braid and for security of connectors.
5. Inspect for physical damage to the printed wiring assemblies.

3.4 POWER REQUIREMENTS

The auto restart loader receives +5VDC and ±12VDC from the processor DC power supply by connection to the assigned backplane board slot position. The stall alarm panel receives +5VDC from the auto restart loader via the auto restart loader paddle board through connection of the stall alarm panel cable. Power for the IOM adapter

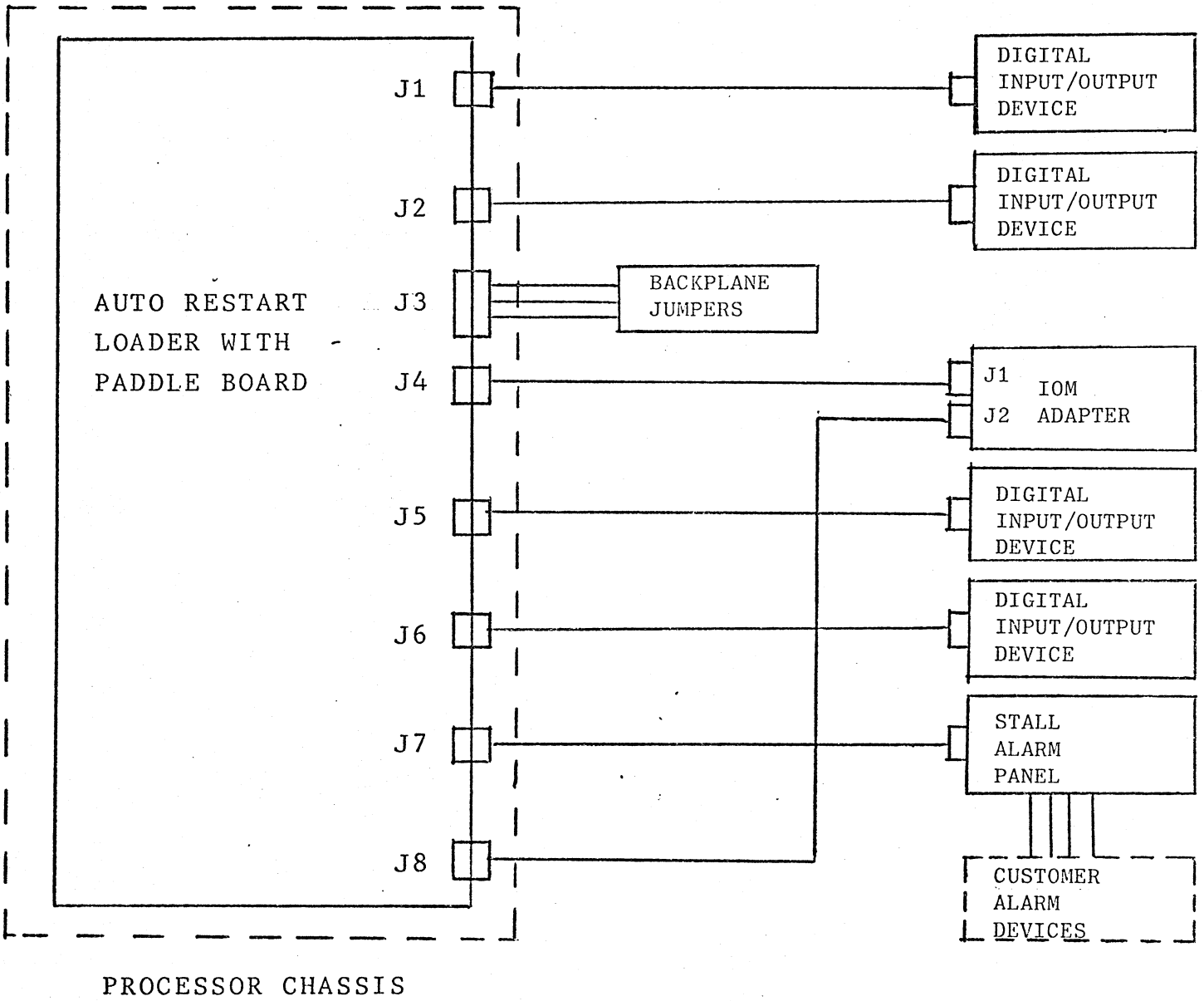


FIGURE 3-1. AUTO RESTART LOADER SYSTEM BLOCK DIAGRAM

3.4 {Continued}

is obtained from the computer interface expander backplane via a jumper wire from the +5VDC terminal to the adapter board. The jumper wire is an integral part of the adapter board.

3.5 PREPARATION OF ARL BOARD

3.5.1 CPU Backplane Wiring

The Auto Restart Loader requires connection of some processor backplane signal lines that are not normally installed. Inspect the backplane for wiring of the signals listed in Table 3-1. If they are not already installed, use the wire wrap tool to install the wiring between the original backplane slots and the auto restart loader board slot {slot C}. Wire used on the backplane should be white 30 AWG {P/N 15006509} or equivalent.

TABLE 3-1. CPU BACKPLANE WIRE CHANGES

SIGNAL NAME	SLOT C PIN	TO SLOT/PIN
SETSM204/	44	K/273
DSDATA/	41	K/248
DSUARTCLK/	42	K/206
MC-S/ {EXMC/}	293	K/74

3.5.2 Switch/Jumper Verification

Prior to installation of the Auto Restart Loader printed wiring assembly into the processor chassis, certain switch, jumper and chip configurations must be established or verified.

CAUTION

Printed wiring assemblies with red solder masks, such as the auto restart loader, contain MOS or electrostatic sensitive devices. Exercise extreme care in handling to avoid damage. Common practices, such as touching a grounded surface before handling, inserting in antistatic or conductive bags for storage or transfer, and repairing only at properly equipped and grounded work stations, must be strictly followed.

3.5.3 Equipment Code Selection

An equipment code of 6 has been assigned for the CYBER 18 Auto Restart Loader applications. This code is established by the four-segment, dual in line package (DIP) switch at PWA location M11, figure 3-2. Refer to Table 3-2 and configure the switch to establish the required equipment code.

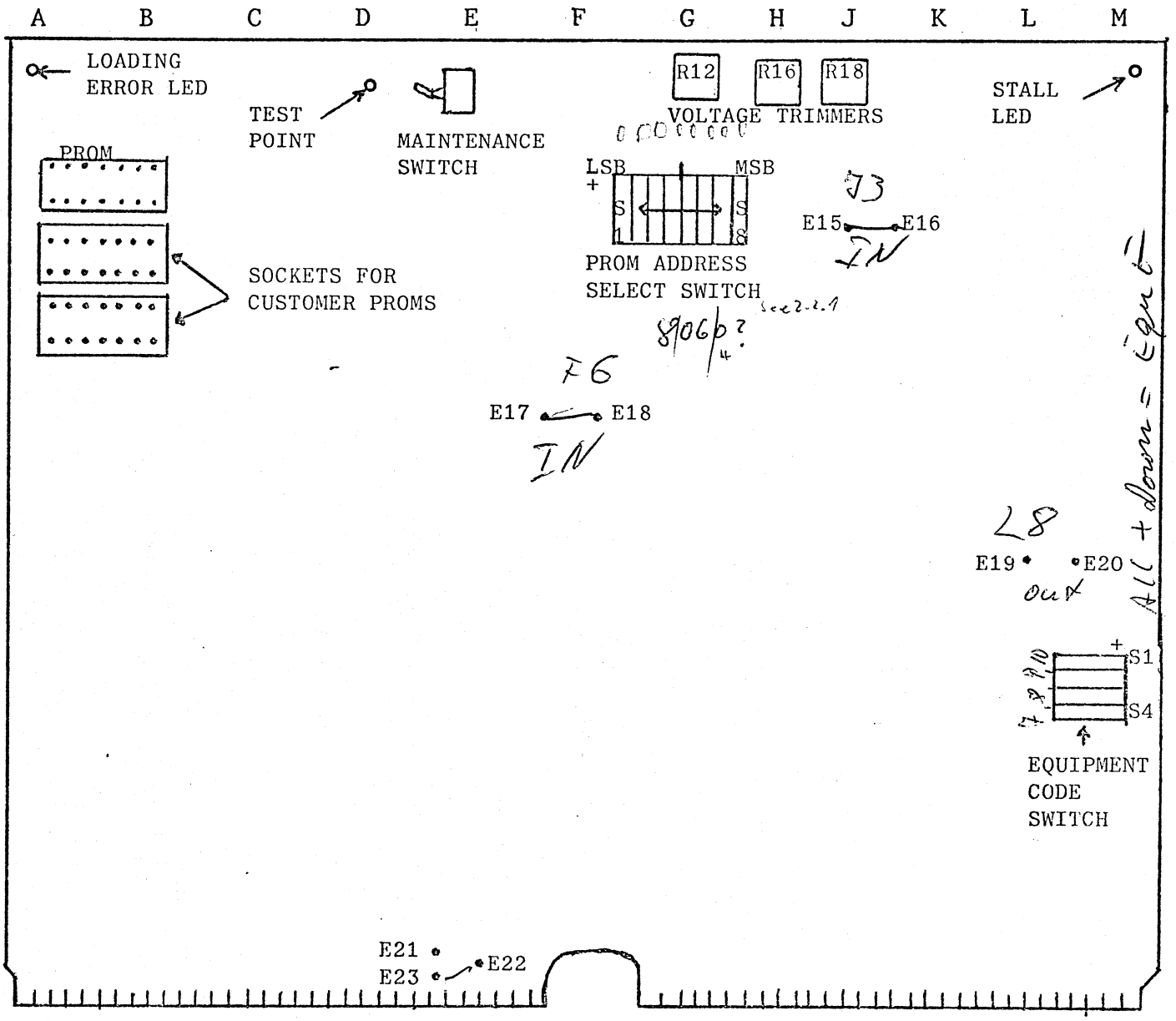


FIGURE 3-2. AUTO RESTART LOADER COMPONENT LOCATION

TABLE 3-2. EQUIPMENT CODE SELECT SWITCH SETTINGS

Equipment Code	Switch Position (Location M11)			
	S1	S2	S3	S4
15	ON	ON	ON	ON
14	ON	ON	ON	OFF
13	ON	ON	OFF	ON
12	ON	ON	OFF	OFF
11	ON	OFF	ON	ON
10	ON	OFF	ON	OFF
9	ON	OFF	OFF	ON
8	ON	OFF	OFF	OFF
7	OFF	ON	ON	ON
6†	OFF	ON	ON	OFF
5	OFF	ON	OFF	ON
4	OFF	ON	OFF	OFF
3	OFF	OFF	ON	ON
2	OFF	OFF	ON	OFF
1	OFF	OFF	OFF	ON
0	OFF	OFF	OFF	OFF

† Normal CYBER 18 Configuration

3.5.4 Load Starting Address

The deadstart loading operation can be initiated by an AQ command. This loading operation does not start from location zero as in the normal restart mode; instead, it starts from a PROM location specified either by the contents of the A register or by the PROM address select switches at PWA location G3 (figure 3-2). The PROM address select switches must be set to establish this optional starting address. A switch segment is considered on (Closed) when the toggle adjacent to the + (plus) mark on the switch is depressed.

.5.5 PWA Jumpers

The signal jumper configuration listed in Table 3-3 must be established on the PWA for operation of the auto restart loader in a CYBER 18 system. The jumper terminal locations are shown in figure 3-2.

TABLE 3-3. AUTO RESTART LOADER PWA JUMPERS

SIGNAL NAME	TERMINALS	BOARD LOCATION	CONFIGURATION
PUP RESTART ENABLE	E15 - E16	J3	IN
DG CLR ON MR	E17 - E18	F6	IN
PROG-PROT/	E19 - E20	L8	OUT
SM204/	E21 - E22	E14	OUT
DSTTL/	E23 - E22	E14	IN

3.5.6 Deadstart Data PROMS

The Auto Restart Loader contains one programmable Read Only Memory (PROM) chip at board location A3, which contains firmware. Two IC sockets at board locations A4 and A5 are provided to mount pre-programmed PROM chips, furnished by the customer, which contain the deadstart data. If these PROMs are provided by the user, install the chips at board locations A4 and/or A5 (figure 3-2) according to the word size defined in Table 3-4.

TABLE 3-4. INCREASED DATA PROM LOCATIONS

Word Size	Socket A4	Socket A5
512 by 8	82S141	Not Used
1024 by 8	82S181	Not Used
2048 by 8	82S191	Not Used
4096 by 8	82S191	82S191

3.6 INSTALLATION

3.6.1 Installation of ARL

3.6.1.1 PWA Insertion

After all switch, jumper, and PROM selections have been determined and properly set, the Auto Restart Loader PWA is ready for insertion into the assigned processor slot. Proceed as follows:

1. Remove the right side panel of the processor cabinet.
2. Release the two captive latches on the processor chassis cover and remove the cover.

CAUTION

The Auto Restart Loader PWA must be installed with its components facing left. Power must be turned off when the PWA is inserted.

3. Carefully insert the board into chassis slot C. Make sure that the board is properly aligned in the upper and lower chassis guide rails.
4. Ensure that the board is fully seated within the chassis backplane connector by applying firm thumb pressure at the upper and lower corners of the front of the board.
5. Replace the chassis cover plate.
6. Replace the cabinet right side panel.

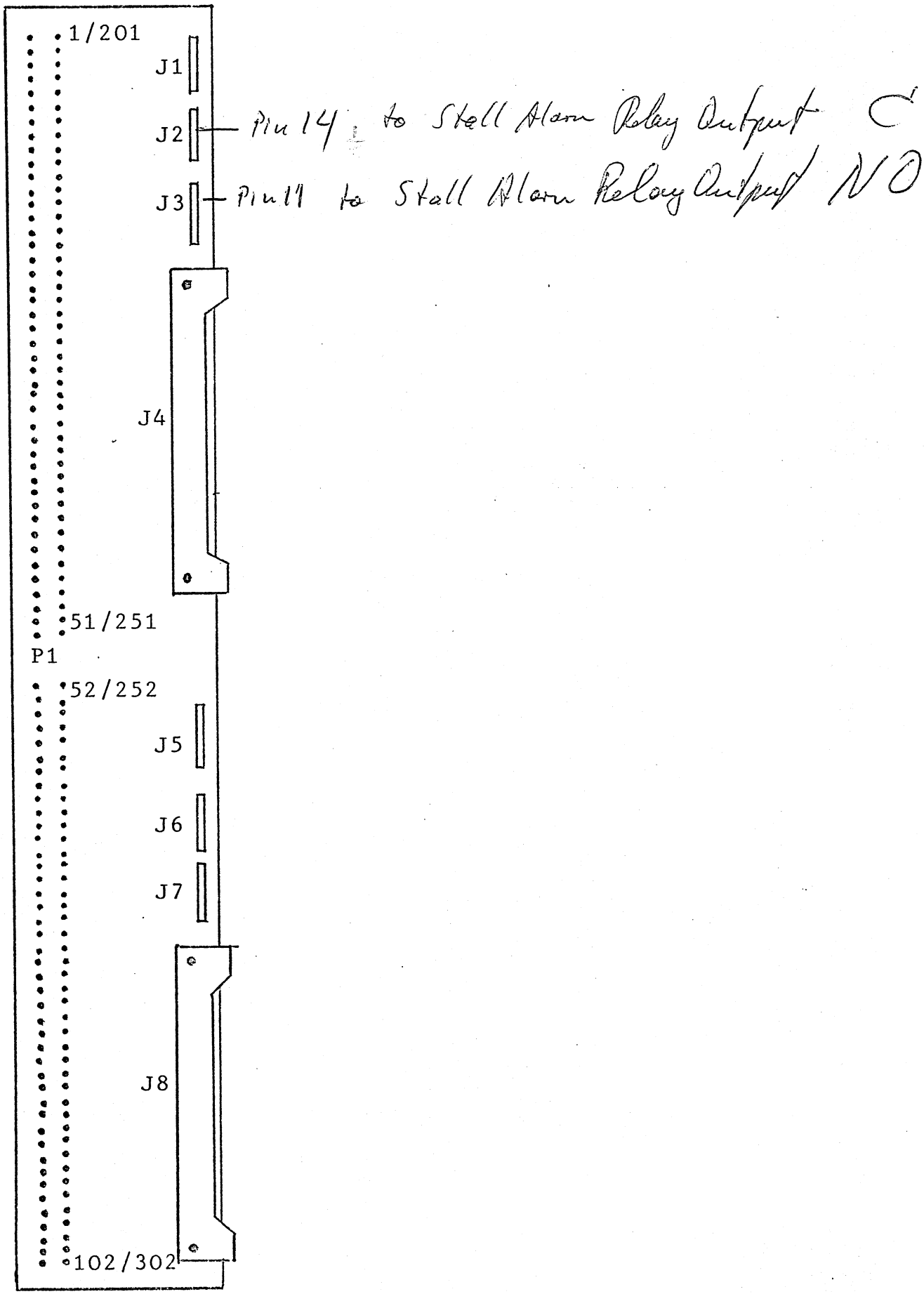


FIGURE 3-3. AUTO RESTART LOADER PADDLE BOARD

3.6.1.2 Paddle Board Installation

The auto restart loader paddle board (figure 3-3) is installed on the processor backplane over the slot C backplane pins. The paddle board provides the connection interface between the auto restart loader and the devices external to the processor. Proceed as follows to install the paddle board.

1. Remove the processor side and rear panels.
2. Attach the paddle board to the slot C backplane pins. Verify as labeled on the paddle board connectors the starting and ending backplane pin numbers to which the paddle board should be securely mated.

3.6.1.3 Paddle Board Jumpers

Additional jumpers must be installed between the auto restart loader paddle board, the processor backplane, and the processor DC power supply.

Eight macro interrupts are made available to the processor from the IOM devices. The interrupts are presented to the auto restart loader paddle board from the IOM devices via the IOM adapter signal cables. These lines must be jumpered from connector J3 of the paddle board to the processor status mode interrupt (SMI) board slot (slot L) if IOM devices are a part of the system. The pin assignments for the interrupt lines at the paddle board are

3.6.1.3 {Continued}

listed in Table 3-5. {Refer to the applicable 1500/IOM device hardware reference/maintenance manual for installing the IOM devices}.

TABLE 3-5. IOM INTERRUPT LINE PIN ASSIGNMENTS

INTERRUPT DESIGNATION	FROM IOM		TO CPU	
	J4	P1	P1	J3
INT1-I/ = 3 (CPU)	9	57	38	8
INT2-I/	11	58	37	7
INT3-I/ = 12	13	59	36	6
INT4-I/ = 15	15	60	35	5
INT5-I/ = 9	17	61	34	4
INT6-I/	19	62	33	3
INT7-I/	21	63	32	2
INT8-I/	23	64	31	1

→ Line 15 CPU

The auto restart loader macro interrupt line and other signals must also be connected to the auto restart loader at connector J3 of the paddle board. Refer to Table 3-6, and install the jumpers and wiring between their origins and connector J3 of the paddle board.

TABLE 3-6. PADDLE BOARD SIGNAL JUMPERS

SIGNAL NAME	SOURCE	DESTINATION
INTERRUPT/	J3-9	Slot L, Pin 271 †††
DSTTL/	J3-10	Customer Equipment †
DSCC/	J3-11	Customer Equipment †
ACFAIL/	J3-13	Processor power supply TB1-4 or battery back-up power supply terminal 4 ††

† These outputs are provided so nonstandard customer equipment can use the auto restart loader deadstart capability.

†† For processors with the battery backup unit.

†††Macro Interrupt 06 - Standard assignments

3.6.2 IOM Adapter

The IOM adapter permits connection of 1500 Series IOM peripherals to the auto restart loader. The IOM adapter consists of one interface printed wiring assembly that is inserted into position 1 of the EL102-A computer interface expander (CIE) and two cable assemblies that connect between the interface PWA and the auto restart loader paddle board. No EL101-A computer interface unit (CIU) is required for this configuration. (Refer to the CIE/CIU hardware reference/maintenance manual for installing the computer interface expander.)

3.6.2 (Continued)

To install the IOM adapter, proceed as follows:

1. Insert the IOM interface printed wiring assembly into position 1 of the computer interface expander.

2. Connect the interface PWA power wire terminal ring to terminal E2 (+5V) on the CIE backplane, as shown in figure 3-4. Route the wire around the left side of the card cage (as viewed from the front) from the PWA to the backplane terminal.

3. Connect one IOM adapter cable A end to J4 of the auto restart loader paddle board. Connect the second IOM adapter cable A end to J8 of the paddle board.

4. Route the two cables through the cable entry panel and out the rear of the processor cabinet to the rear or side entry of the vertical cabinet. Continue routing the cable to the front of the vertical cabinet, passing the left side (as viewed from the front) of the computer interface expander chassis, and right to the IOM interface PWA.

5. Connect the cable from J4 of the paddle board to J1 of the interface PWA. Connect the cable from J8 of the paddle board to J2 of the interface PWA, as shown in figure 3-4.

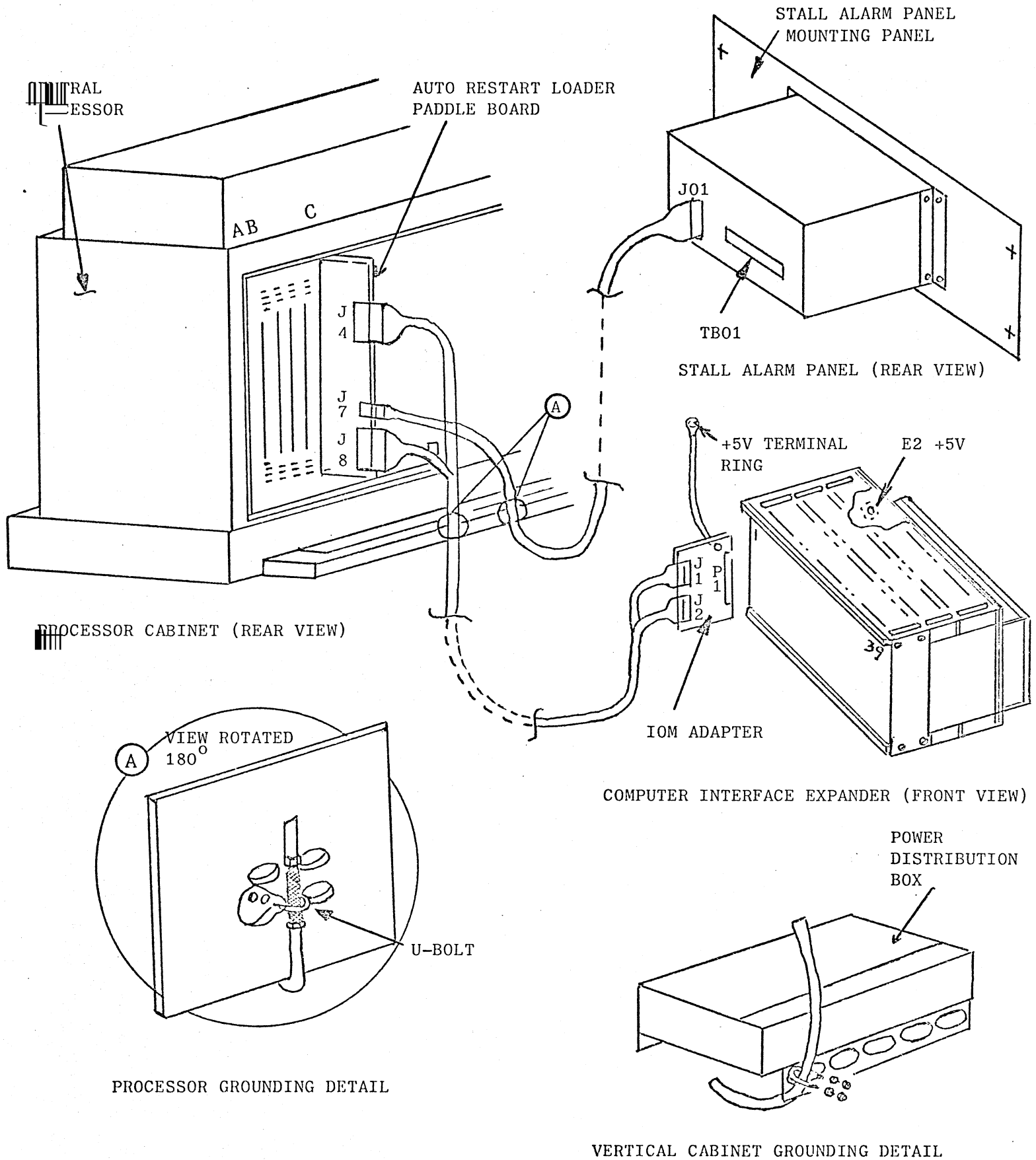


FIGURE 3-4. AUTO RESTART LOADER SIGNAL CABLING

3.6.2 (Continued)

6. As shown in the grounding details of figure 3-4, install one U-bolt around each end of the signed cables at the shield braid. Attach the U-bolts to the cable entry panels. More than one cable may occupy a U-bolt.

3.6.3 Stall Alarm Panel

The stall alarm panel has a removable mounting panel that allows mounting in a 19-inch (483-millimeter) RETMA rack position of the vertical cabinet or can be removed to allow desk top operation. Connection of the stall alarm panel to the auto restart loader paddle board is via one signal cable supplied with the panel. Connection to the stall alarm panel of external devices is via a terminal block on the rear of the stall alarm panel. Table 3-7 lists the connections available for external equipment to interface with the stall alarm panel.

To install the stall alarm panel, proceed as follows:

1. Install the panel, with the mounting panel attached, into the top position of the vertical cabinet on the RETMA rails; or remove the mounting panel if desk top installation is desired.
2. Connect the stall alarm panel cable assembly A end to J7 of the auto restart loader paddle board, as shown in figure 3-4.

TABLE 3-7. STALL ALARM PANEL TB01 CONNECTIONS

TERMINAL NUMBER	SIGNAL	DESCRIPTION
1	Relay 1 NO	Relay 1 normally open contact
2	Relay 1 C	Relay 1 common contact
3	Relay 1 NC	Relay 1 normally closed contact
4	Relay 2 NO	Relay 2 normally open contact
5	Relay 2 C	Relay 2 common contact
6	Relay 2 NC	Relay 2 normally closed contact
7 †	+FLDS	Field stall positive input
8 †	+FLDS	Field stall positive input
9 ††	-FLDS	Field stall ground input
10 ††	-FLDS	Field stall ground input

† Pins 7 and 8 are jumpered together internally.

†† Pins 9 and 10 are jumpered together internally.

3.6.3 (Continued)

3. Route the cable through the processor cable entry panel and out the rear of the processor cabinet to the rear or side entry of the vertical cabinet or to the intended location of the stall alarm panel if it is not located in the vertical cabinet.
4. If the panel is to be located in the vertical cabinet, continue routing the cable under the power distribution box and up the right side (as viewed from the front) of the cabinet to the stall panel.

3.6.3 (Continued)

5. Connect the B end of the cable assembly to J01 of the stall alarm panel.
6. As shown in the grounding details of figure 3-4, install one U-bolt around each end of the signal cable at the shield braid. Attach the U-bolts to the cable entry panels of the cabinets. More than one cable may occupy a U-bolt. If the panel is not installed in the vertical cabinet, a suitable grounding of the shield braid at the panel end of the cable must be accomplished.
7. Connect any customer-supplied external alarm devices to the stall alarm panel terminal block according to Table 3-6.

3.6.4 Digital I/O Devices

If additional I/O devices are to be controlled by the auto restart loader, the device signal cables are connected to paddle board connectors J1, J2, J5 and J6 (figure 3-3). The signal cables to the I/O devices are not supplied with the auto restart loader.

To connect the I/O device signal cables, proceed as follows:

1. Attach the signal cable to the appropriate connector of the auto restart loader paddle board. (Refer to figures 3-1 and 3-4.)

TABLE 3-8. DIGITAL I/O DEVICE CONNECTIONS

CONNECTOR	BYTE MODE	WORD MODE	NOTE
J1	Byte 0	Word 0 LSB	Control signals Not used in Word Mode
J2	Byte 1	Word 0 MSB	
J5	Byte 2	Word 1 LSB	Control signals Not used in Word Mode
J6	Byte 3	Word 1 MSB	

NOTE: LSB - Least Significant Byte
MSB - Most Significant Byte

3.6.4 {Continued}

2. Route the cable through the processor cable entry panel and out the rear of the processor cabinet to the appropriate connector for the I/O device. {Refer to the applicable hardware maintenance manual for installing the I/O device.}
3. All signal cable shield braids must be grounded at the processor cable entry panel using U-bolts, as shown in the grounding detail of figure 3-4. More than one cable may occupy a U-bolt.

3.6.4 4. Accomplish suitable signal cable shield braid grounding at the I/O device.

5. Replace all panels removed to accomplish installation of the auto restart loader and associated equipment.

3.7 DIAGNOSTIC TESTING

Perform the manual operating and diagnostic checks according to the diagnostic decision logic tables (DDLTs) described in the applicable subsystem hardware maintenance manual.

NOTE

The diagnostic tests and routines described in the subsystem hardware maintenance manual can be performed only after the processor, console display, and flexible disk drive or tape cassette (diagnostic load level device) installations are complete.

NOT APPLICABLE

DIAGRAMS

5.1 GENERAL

This section contains the following diagrams:

Title

- ARL (B1) Logic Diagram (P/N 96870580)
- ARL (B2) Logic Diagram (P/N 96751079)
- ARL Paddle Board Wiring Diagram (P/N 96752621)
- Stall Panel Wiring Diagram (P/N 88861300)
- IOM Adapter Logic Diagram (P/N 96751052)

		101	102	103	104	105	106	107	108	109	110	111	112	113	114	115	116	117	118	119	120	GATES USED	GATES PER IC	IC's REQ'D	SPARE GATES
74LS00 1514900	14		1				1	PKG III				PKG							1			16	4	4	0
74LS02 1514500	14		1				III		IIII			1										8	4	2	0
7403 9674154	14						II	I												PKG PKG PKG I		19	4	5	+1
74LS04 1514510	14	I	III	II			PKG II	PKG III				II							II	PKG PKG PKG I	IIII	45	6	8	+3
74 04 8892450	14	IIII	PKG											I	I	I	I					12	6	2	0
74LS05 1514530	14																				PKG I	6	6	1	0
74LS08 1514598	14		1	II			II					1							H			8	4	2	0
74LS10 1514560	14		1				1	II														4	3	2	+2
74LS11 1514570	14		1				II	I														4	3	2	+2
74LS20 1514530	14			I			II	I														4	2	2	0
74LS30 1514610	14								I													1	1	1	0
74LS32 1514620	14		IIII				III	III														10	4	3	+2
74LS74	14		1	II			IIII	III					PKG III						IIII		1	23	2	12	+1
74LS86 1514640	14										PKG PKG PKG I	PKG PKG PKG I	PKG III									40	4	10	0
74LS138 1514740	16		1																			1	1	1	0
74LS139 1514660	16							I														2	1	2	0
74LS151 1516330	16						I															1	1	1	0
74LS174 1514750	16		1				1					1										3	1	3	0
74LS175 1514690	16									IIII				II	II	II	II					12	1	12	0
74LS193 1514700	16		III	I																		4	1	4	0
74LS253 1514720	16					III																4	1	4	0
75461	8												IIII	PKG III	PKG III	PKG III	PKG III					36	2	18	0
8T97 3891880	16		1					1			PKG PKG PKG I	1							PKG PKG PKG I	PKG PKG PKG I	PKG PKG PKG I	67	6	12	+5
8T98 8892090	16							I													PKG PKG III	15	6	3	+3
8111A 1515160	8			II																		2	1	2	0
8123 8889400	16	IIII					I	II	PKG	II		IIII										18	1	18	0
8212 1515540	24		1													I						1	1	1	0
8214	24		1																			1	1	1	0
8216 1515530	16									II												2	1	2	0
9255A	40											1										1	1	1	0
8251B/ 8251	28			I														II				3	1	3	0
LM 339	14			PKG I																		6	4	2	+2
MC1489A 3818C501	14		1										PKG III	PKG III	PKG III	PKG III	PKG III					41	4	11	+3
TRIGOLA 2008B1DC	40																		1			1	1	1	0
Z80A 1514320	40	1																				1	1	1	0
DIODE ARRAY	8																								
SOCKETS	28																								
TERMINATOR QUAD ARRAY 5113244	24																								

189

6PIN CERAMIC ONLY

* NOT INCLUDING TEST FEATURE

SOCKETS 1815360

NOT 1815360

PLASTIC DIP

* DENOTES SOCKETS ONLY.

2. ALL DIODES ARE FSA 2619M (DIODE ARRAY)

1. LIST OF SPARE GATES

8T97	(1) @ M8
74LS02	(3) @ A6/7
7403	(1) @ L11
7404	(1) @ L1
74LS04	(2) @ A13, (1) @ G13, (1) @ S13
74LS32	(1) @ M7, (1) @ K10
74LS74	(2) @ M10
LM339	(2) @ J1
MC1489A	(3) @ J4

NOTES: UNLESS OTHERWISE SPECIFIED

8JHT

REVISION RECORD						
REV	ECO	DESCRIPTION	DFT	DATE	CHK	APPD
01	DS18964	[illegible]	BH	8-31-78	G L	AW

	SMALL COMPUTER DEVELOPMENT DIVISION		
DR	B Hall	6-29-78	
CHK	G. LAGE	7-31-78	
ENGR	C Lee	8-16-8	
MFG			
APPD			

TITLE: LOGIC DIAGRAM - AUTO-RESTART LOADER

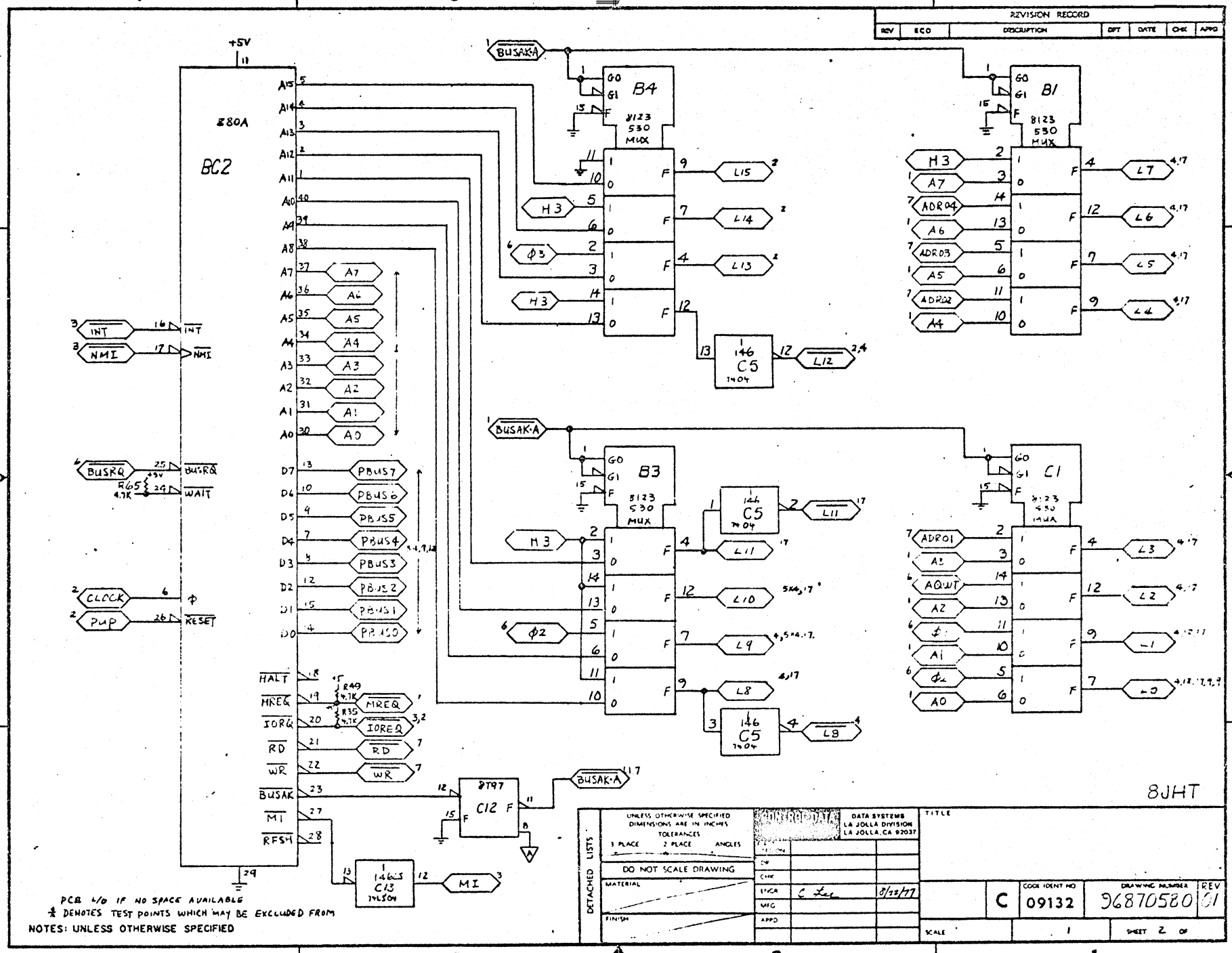
SIZE	CODE IDENT NO.	DRAWING NUMBER
C	09132	96870580

SCALE: NONE | PWA 96870180 PWA 96870380 | SHEET 1 OF 2

96751079 B

3 4 3 2 1

D C B A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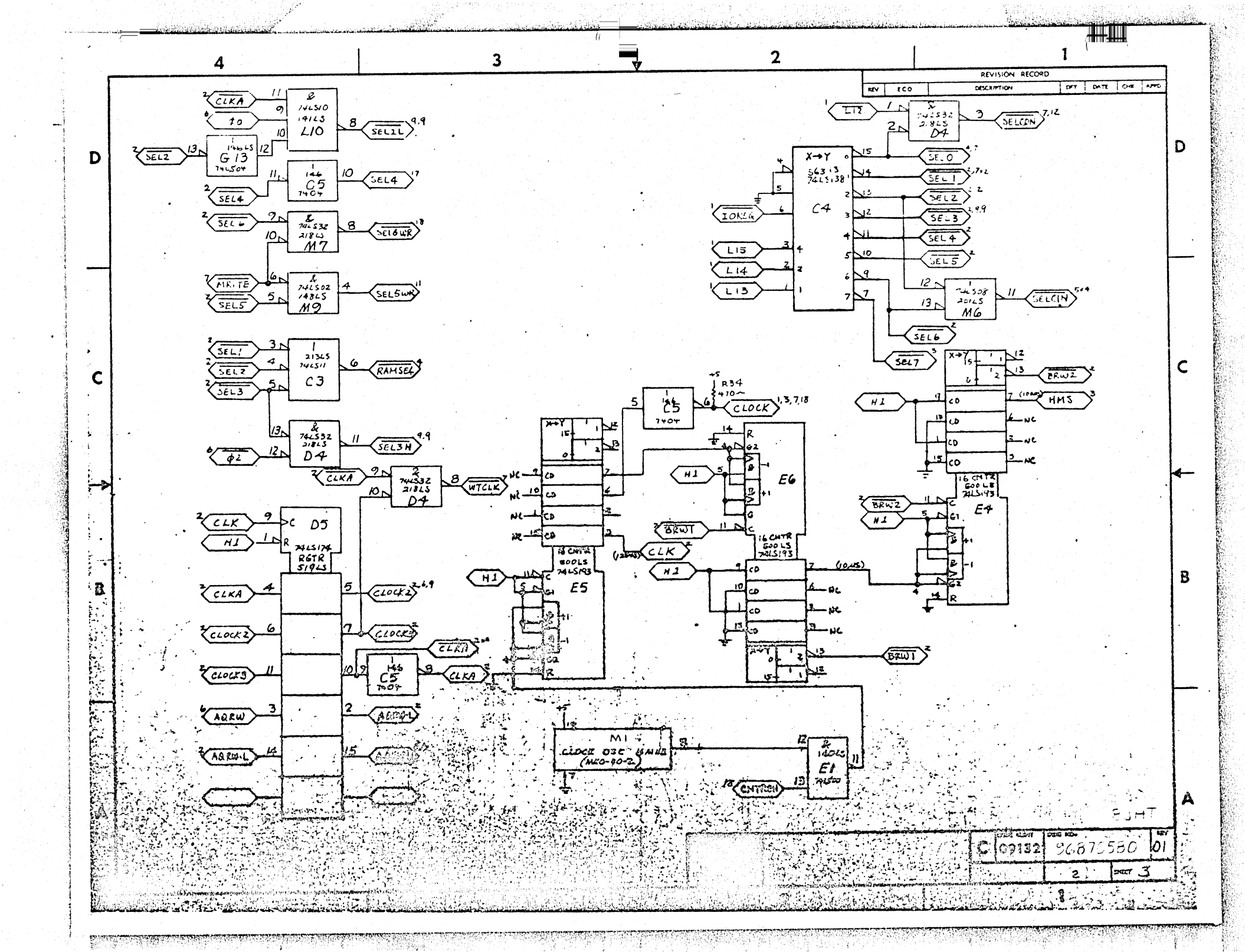
D7 D6 D5 D4 D3 D2 D1 D0
INT
NMI
BUSRQ
WAIT
CLOCK
PUP
RESET
HALT
MREQ
IORQ
RD
WR
BUSAK
M1
RFSH
R65 4.7K
R49 4.7K
R35 4.7K
B4
B1
B3
C1
8123 530 MUX
C5 7404
8T97 C12
146 C13 74LS04
BUSAK-A
H3
A7
A6
A5
A4
A3
A2
A1
A0
ADR04
ADR03
ADR02
ADR01
AQWT
L15
L14
L13
L12
L11
L10
L9
L8
L7
L6
L5
L4
L3
L2
L1
L0
PCB L/O IF NO SPACE AVAILABLE
‡ DENOTES TEST POINTS WHICH MAY BE EXCLUDED FROM
NOTES: UNLESS OTHERWISE SPECIFIED
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
3 PLACE 2 PLACE ANGLES
DO NOT SCALE DRAWING
MATERIAL
FINISH
DETACHED LISTS
DATA SYSTEMS
LA JOLLA DIVISION
LA JOLLA, CA 92037
DRN
CHK
ENGR C. Lee 8/22/77
MFG
APPD
TITLE
8JHT
C
CODE IDENT NO 09132
DRAWING NUMBER 96870580
REV 01
SCALE 1
SHEET 2 OF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ECO
DESCRIPTION
DFT
DATE
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APPD
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SEL1L
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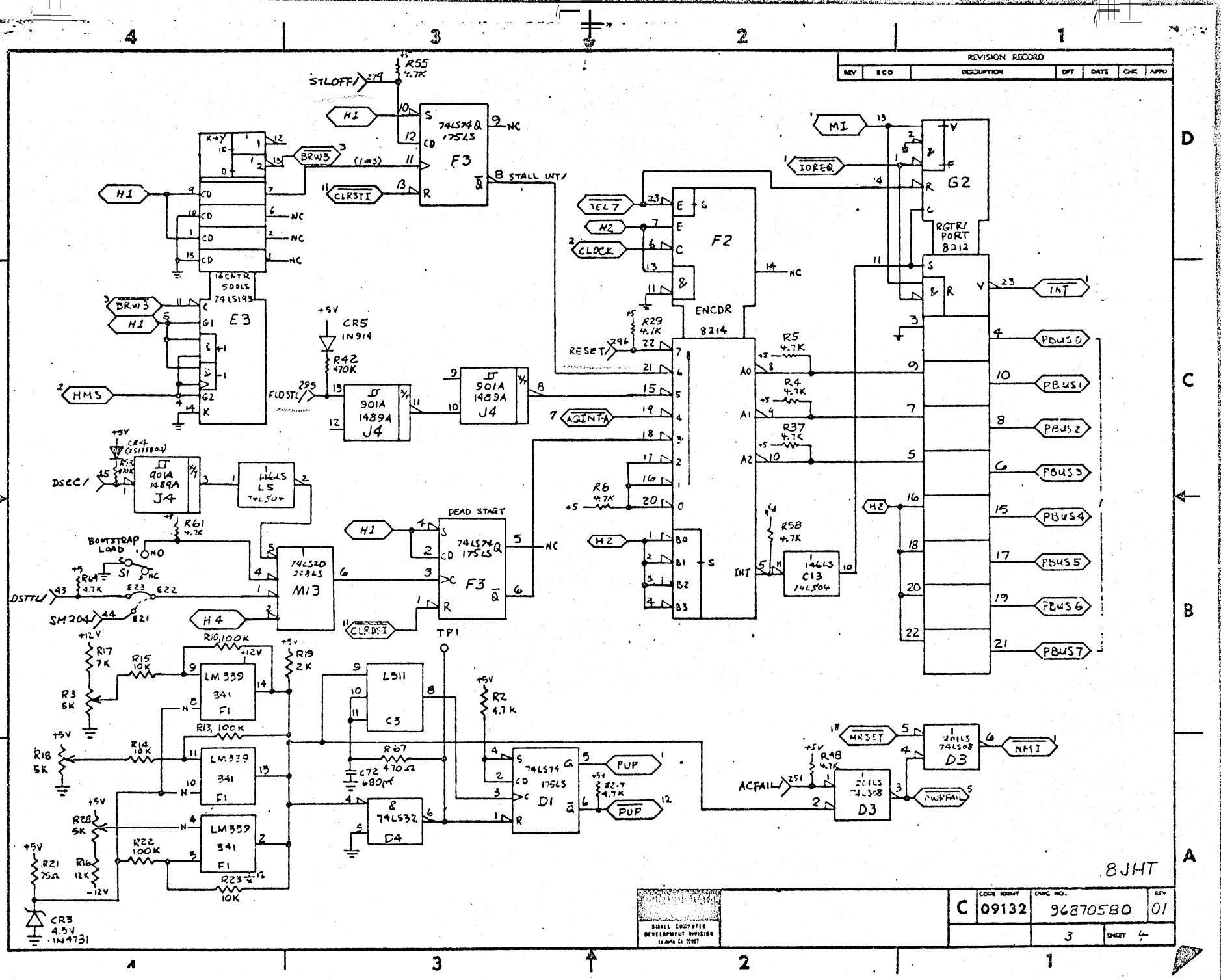
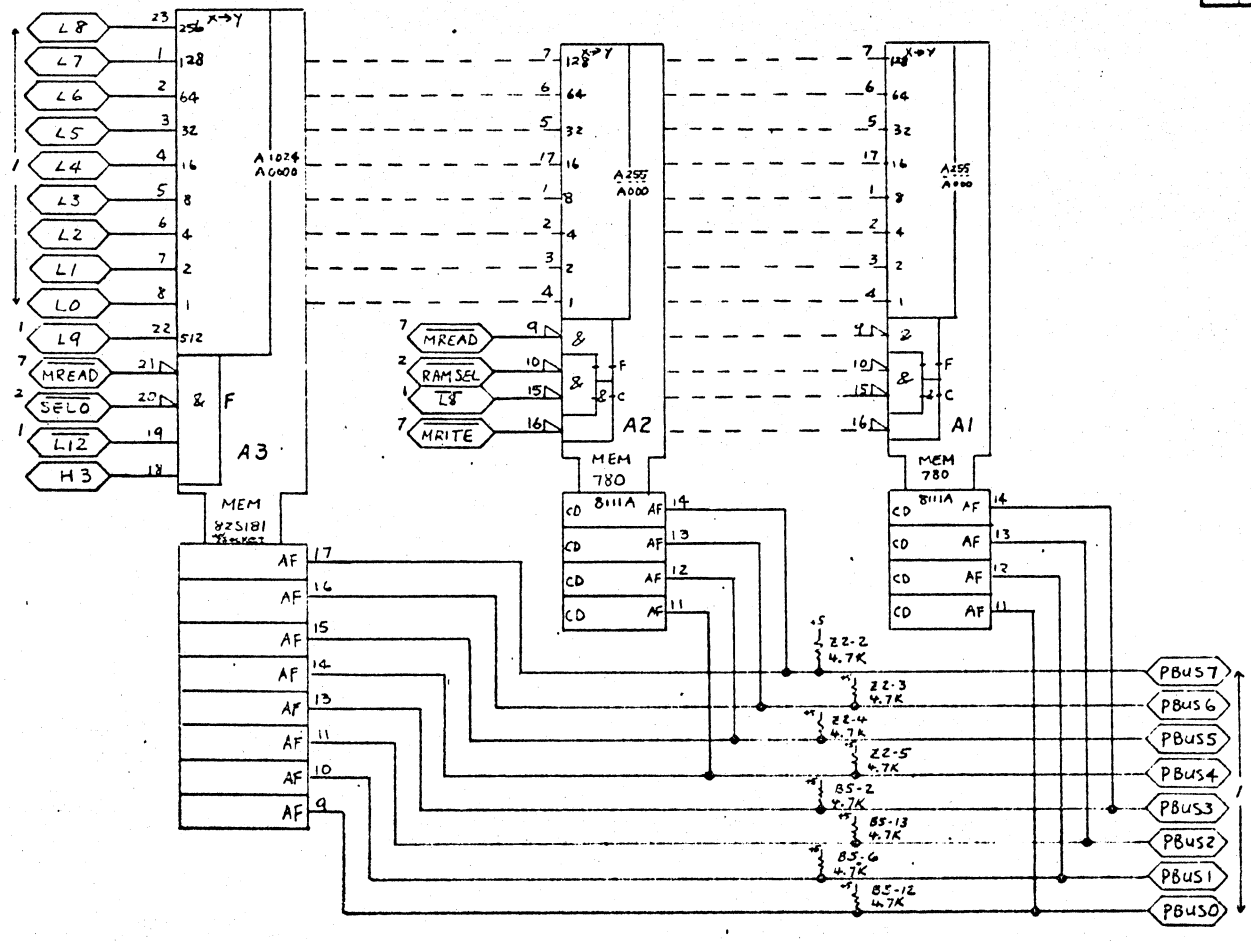
C5
SEL4
SEL6
M7
SEL6WR
MR.TE
SEL5
M9
SEL5WR
SEL1
SEL2
SEL3
C3
RAMSEL
φ2
D4
SEL3H
WTCLK
D5
CLK
H1
CLOCK2
CLOCK3
AQRW
AQRW-L
C4
IORLG
L15
L14
L13
SEL0
SEL1
SEL2
SEL3
SEL4
SEL5
SEL6
SEL7
M6
SELCIN
L12
SELCON
R34
CLOCK
E6
E5
E4
BRW1
BRW2
HMS
M1
CLOCK DRIVER (MEG-90-2)
E1
CNTRSH
C
09132
96875580
01
2
3


REVISION RECORD
REV
ECO
DESCRIPTION
DFT
DATE
CHK
APPD
STLOFF/
R55 4.7K
H1
74LS74Q 17SLS F3
STALL INT/
NC
BRW3
CLR3TI
16CNTR 50DLS 74LS193 E3
HMS
CR5 IN914
R42 470K
FLOSTL/
901A 1489A J4
DSECI/
CR4 (2S1T800)
74LS20 20DLS M13
DEAD START
DSTTL/
SH204/
BOOTSTRAP LOAD
SI
R61 4.7K
H4
CLRDSI
TP1
R7 7K
R15 10K
R3 5K
R10 100K
R19 2K
LM339 341 F1
R18 5K
R14 10K
R13 100K
R28 5K
R22 100K
R16 12K
R21 75Ω
R23 10K
CR3 4.5V 1N4731
L511 C3
R67 470Ω
C72 680pf
74LS32 D4
R2 4.7K
74LS74 D1
PUP
PUF
82.7 4.7K
MI
IOREQ
G2
RQTR/ PORT 8212
INT
PBUS0
PBUS1
PBUS2
PBUS3
PBUS4
PBUS5
PBUS6
PBUS7
JEL7
H2
CLOCK
F2
ENCDR 8214
RESET/
R29 4.7K
AGINT/
R5 4.7K
R4 4.7K
R37 4.7K
R6 4.7K
R58 4.7K
C13 74LS04
MRSET
R48 4.7K
ACFAIL
D3
NMI
PWRFAIL
8JHT
SMALL COMPUTER DEVELOPMENT DIVISION
C
09132
96870580
01
3
SHEET 4



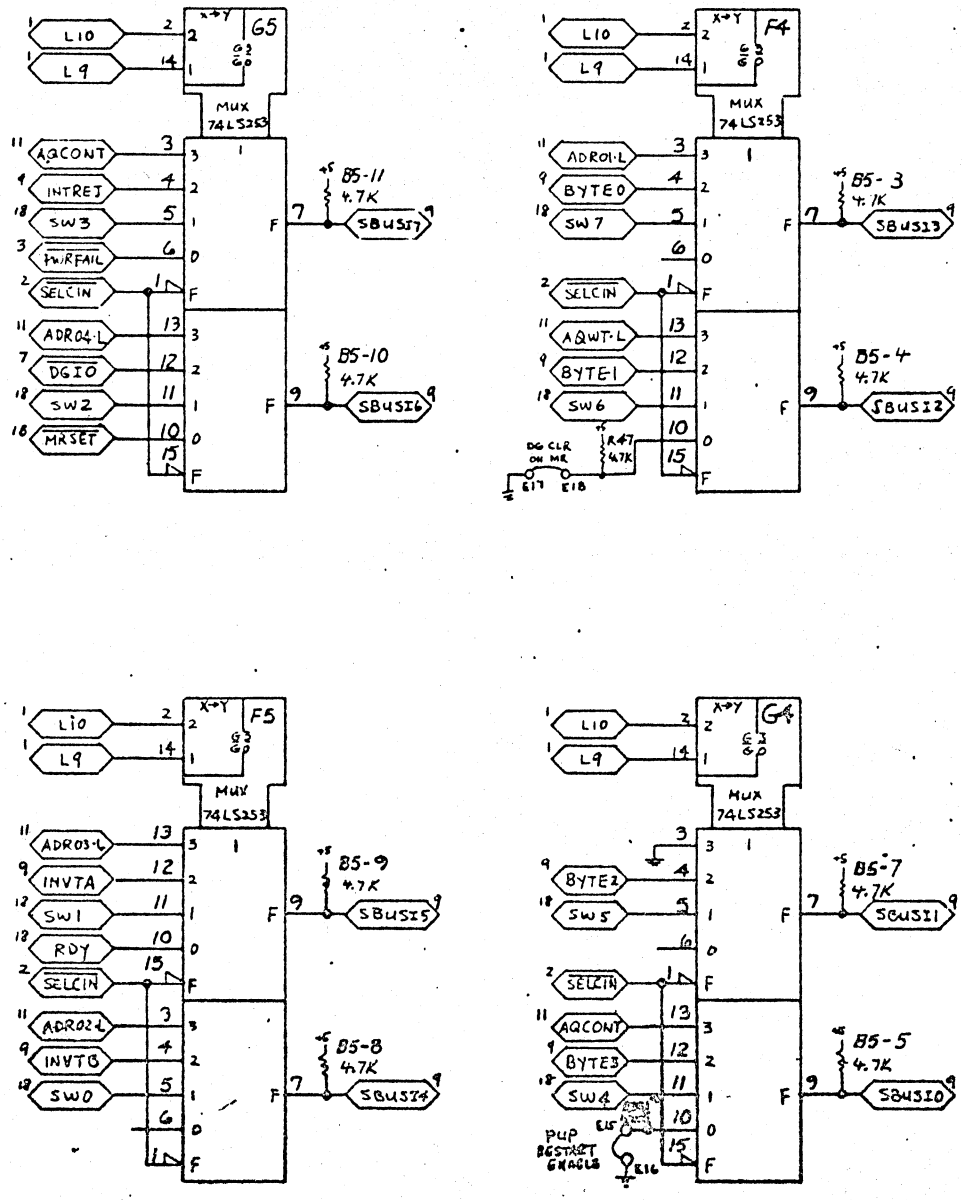
REVISION RECORD

REV	ECO	DESCRIPTION	DFT	DATE	CHK	APPD

8JHT

C	CODE IDENT 09132	DWG NO. 9870580	REV 01
		4	SHEET 5

BOOLL COMPUTER DEVELOPMENT DIVISION



LOGIC TYPE 8JHT

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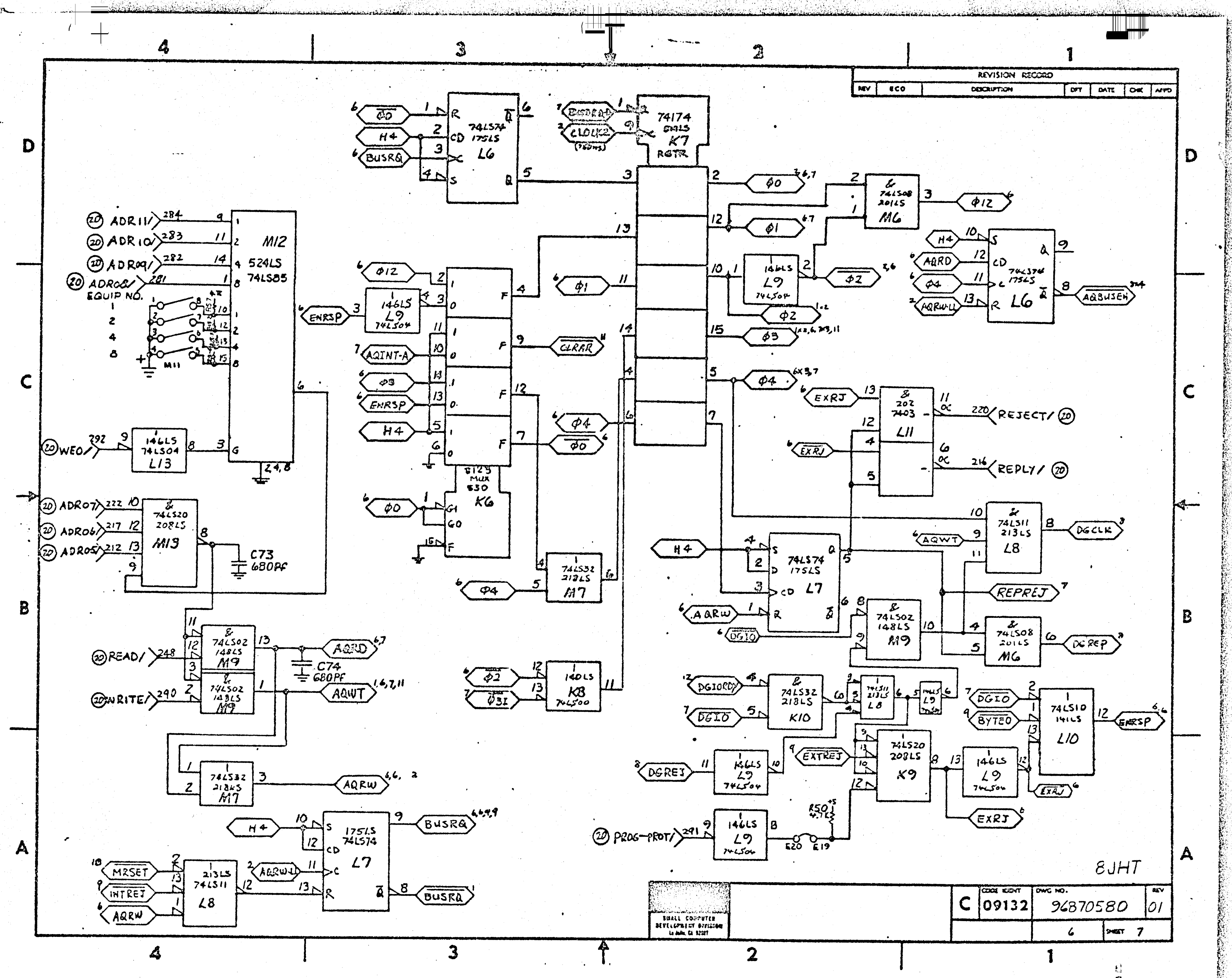
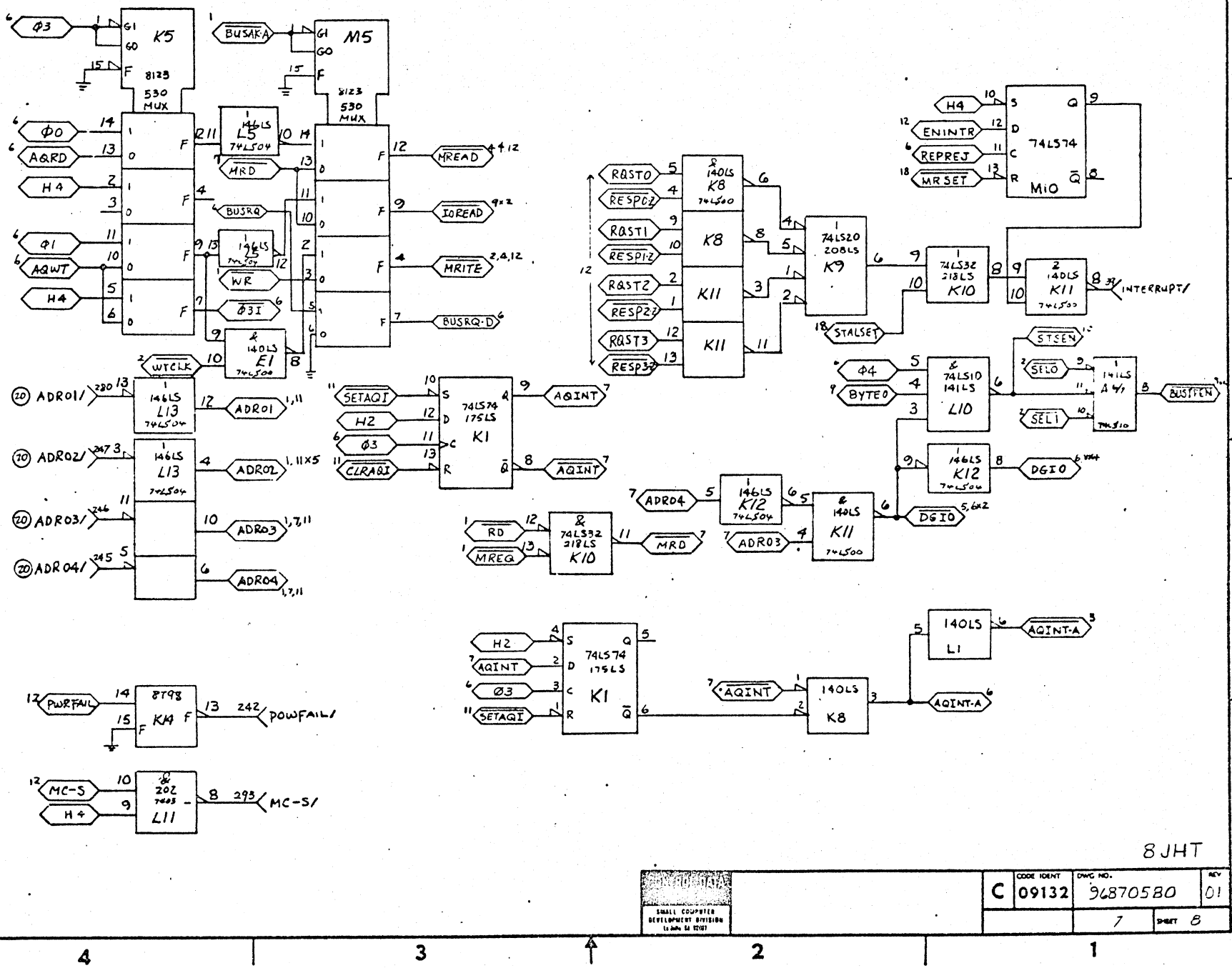
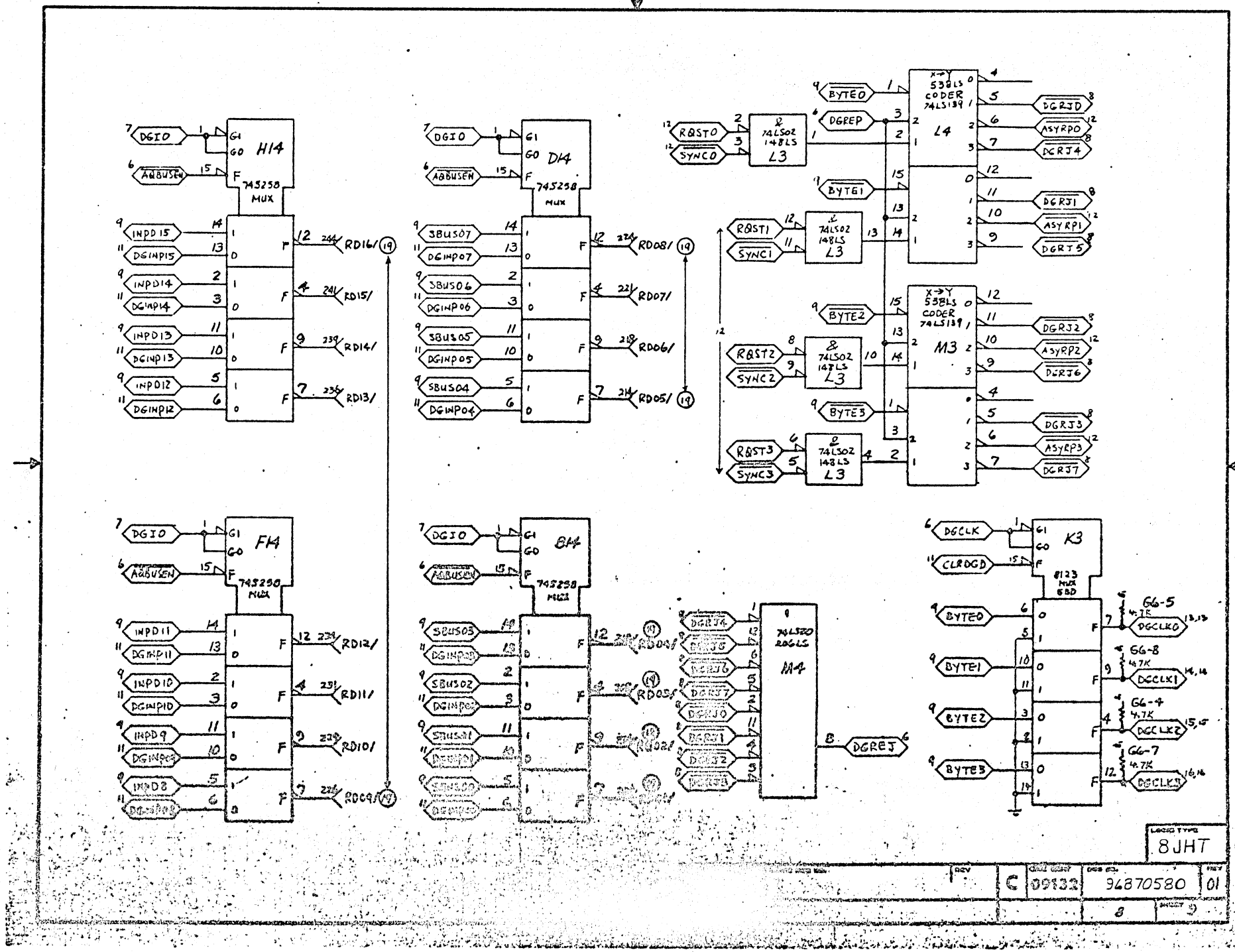
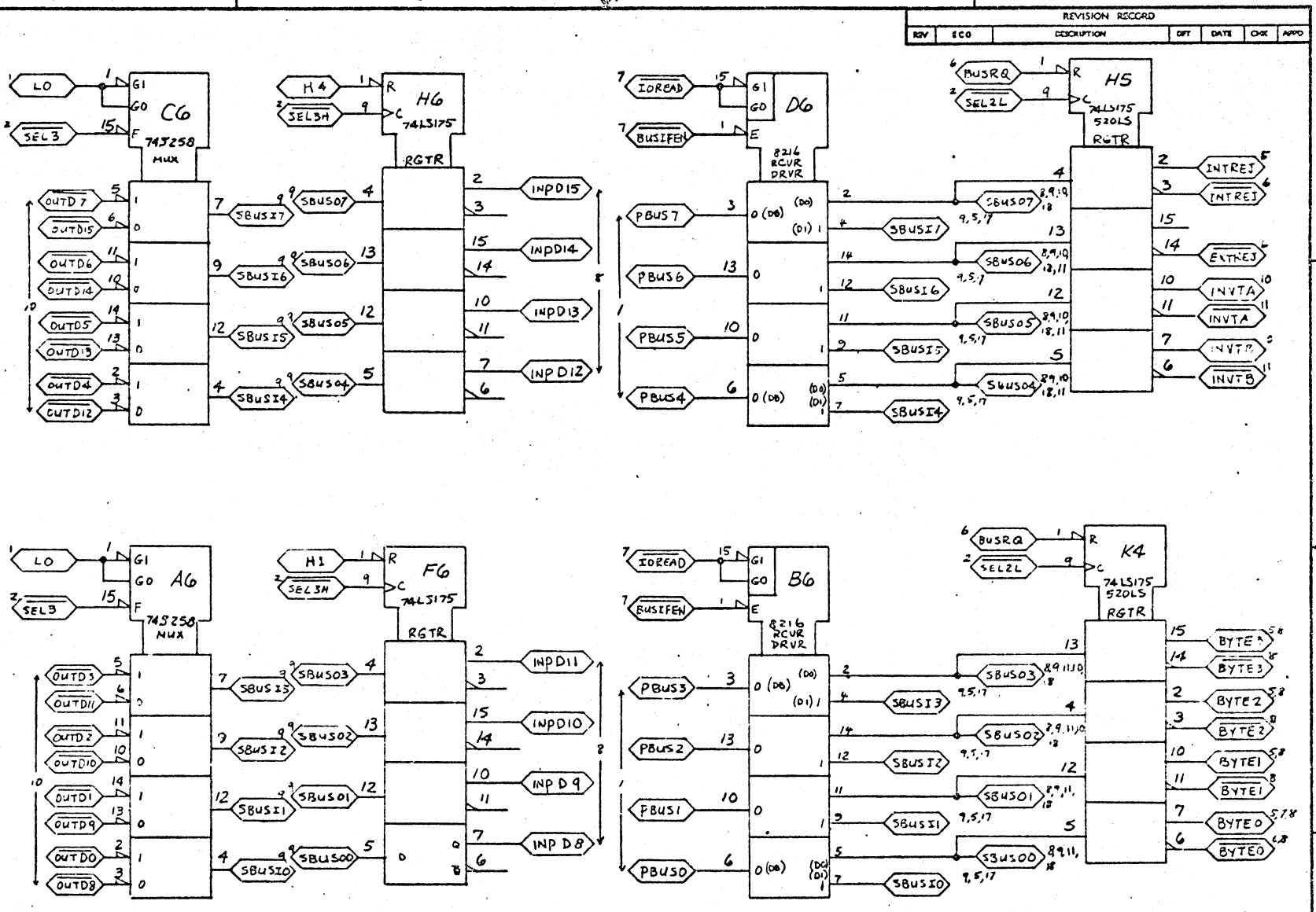
	SHEET				5	SHEET 6



REVISION RECORD
REV
ECO
DESCRIPTION
DFT
DATE
CHK
APPD
74LS74 175LS L6
74174 K7 RGTR
M12 524LS 74LS85
ADR11/
ADR10/
ADR09/
ADR08/
EQUIP NO.
M11
WE0/
146LS 74LS04 L13
ADR07/
ADR06/
ADR05/
74LS20 208LS M19
C73 680PF
ENRSP
146LS L9 74LS04
AQINT-A
H4
8125 MUX 530 K6
CLRAR
74LS32 218LS M7
74LS08 201LS M6
74LS74 175LS L6
AQBUSEN
REJECT/
REPLY/
EXRJ
202 7403 L11
74LS11 213LS L8
DGCLK
AQWT
74LS74 175LS L7
REPREJ
AQRW
DGIO
74LS02 148LS M9
DGREP
DGIORDY
74LS32 218LS K10
140LS K8 74LS00
74LS10 141LS L10
BYTEO
EXTREJ
74LS20 208LS K9
DGREI
PROG-PROT/
R50 4.7K
E20
E19
READ/
WRITE/
74LS02 148LS M9
C74 680PF
AQRD
AQWT
AQRW
BUSRQ
175LS 74LS74 L7
MRSET
INTREJ
213LS 74LS11 L8
SMALL COMPUTER DEVELOPMENT DIVISION
8JHT
C
CODE IDENT 09132
DWG NO. 96870580
REV 01
6
SHEET 7


REVISION RECORD
REV
ECO
DESCRIPTION
DFT
DATE
CHK
APPD
Φ3
K5
8123
530 MUX
BUSAKA
M5
Φ0
AQRD
H4
Φ1
AQWT
WTCLK
L5
L13
L11
K8
K11
K9
K10
K12
K1
K4
M10
E1
MRD
BUSRQ
WR
MREAD
IOREAD
MWRITE
BUSRQ·D
RQST0
RESP0Z
RQST1
RESP1Z
RQST2
RESP2Z
RQST3
RESP3Z
74LS20
20BLS
74LS32
21BLS
140LS
74LS74
17SLS
74LS10
14LS
74LS04
74LS00
ENINTR
REPREJ
MRSET
STALSET
INTERRUPT/
STSEN
SEL0
SEL1
BUSTEN
BYTE0
ADR01/
ADR02/
ADR03/
ADR04/
ADR01
ADR02
ADR03
ADR04
SETAQI
CLRAQI
AQINT
RD
MREQ
DGI0
PWRFAIL
POWFAIL/
MC-S
MC-S/
AQINT-A
8JHT
SMALL COMPUTER DEVELOPMENT DIVISION
C
09132
96870580
01
7
8


H14
D14
F14
B14
M4
K3
L4
M3
74LS258 MUX
74LS02 14BLS L3
74LS138 CODER
74LS240 20BLS
8123 MUX 6BD
DGIO
ABBUSEN
INPD15
DGINP15
INPD14
DGINP14
INPD13
DGINP13
INPD12
DGINP12
INPD11
DGINP11
INPD10
DGINP10
INPD9
DGINP09
INPD8
DGINP08
SBUS07
DGINP07
SBUS06
DGINP06
SBUS05
DGINP05
SBUS04
DGINP04
SBUS03
DGINP03
SBUS02
DGINP02
SBUS01
DGINP01
SBUS00
DGINP00
RD16/
RD15/
RD14/
RD13/
RD12/
RD11/
RD10/
RD09/
RD08/
RD07/
RD06/
RD05/
RD04/
RD03/
RD02/
RD01/
RD00/
RQST0
SYNC0
RQST1
SYNC1
RQST2
SYNC2
RQST3
SYNC3
BYTE0
BYTE1
BYTE2
BYTE3
DGREP
DGRJ0
DGRJ1
DGRJ2
DGRJ3
DGRJ4
DGRJ5
DGRJ6
DGRJ7
DGREJ
ASYRP0
ASYRP1
ASYRP2
ASYRP3
DGCLK
CLRDGD
DGCLK0
DGCLK1
DGCLK2
DGCLK3
G6-5
G6-8
G6-4
G6-7
4.7K
8JHT
C
09132
96870580
01


REVISION RECORD
REV | ECO | DESCRIPTION | DFT | DATE | CHK | APPD
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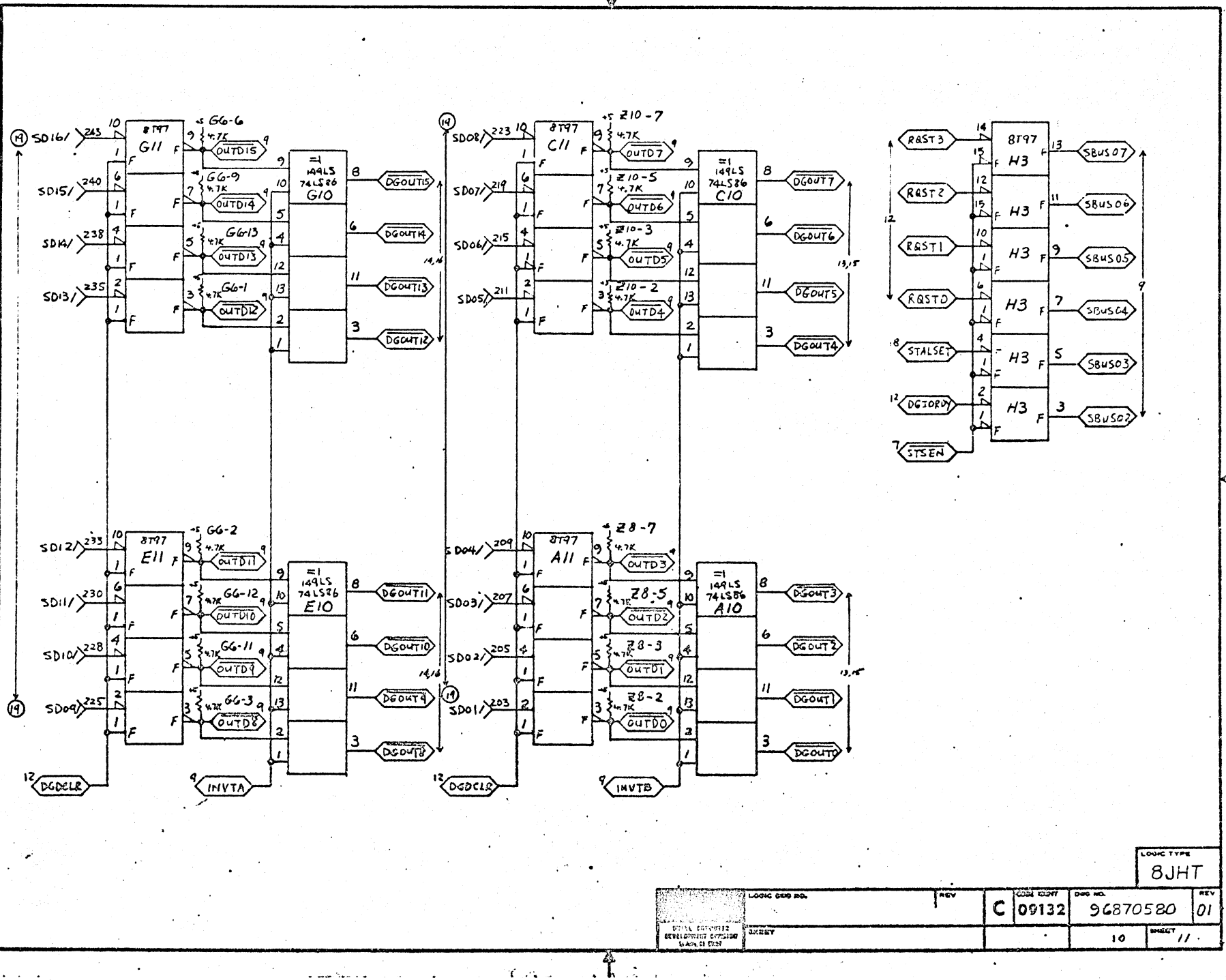
SEL3
C6
74S258
MUX
H4
SEL3H
H6
74LS175
RGTR
OUTD7
OUTD15
OUTD6
OUTD14
OUTD5
OUTD13
OUTD4
OUTD12
SBUSI7
SBUSI6
SBUSI5
SBUSI4
SBUS07
SBUS06
SBUS05
SBUS04
INPD15
INPD14
INPD13
INPD12
IOREAD
BUSIFEN
D6
8216
RCVR
DRVR
PBUS7
PBUS6
PBUS5
PBUS4
SBUSI1
SBUSI6
SBUSI5
SBUSI4
SBUS07
SBUS06
SBUS05
SBUS04
BUSRQ
SEL2L
H5
74LS175
S20LS
RGTR
INTREJ
INTREJ
ENTREJ
INVTA
INVTA
INVTB
INVTB
LO
SEL3
A6
74S258
MUX
H1
SEL3H
F6
74LS175
RGTR
OUTD3
OUTD11
OUTD2
OUTD10
OUTD1
OUTD9
OUTD0
OUTD8
SBUSI3
SBUSI2
SBUSI1
SBUSI0
SBUS03
SBUS02
SBUS01
SBUS00
INPD11
INPD10
INPD9
INPD8
IOREAD
BUSIFEN
B6
8216
RCVR
DRVR
PBUS3
PBUS2
PBUS1
PBUS0
SBUSI3
SBUSI2
SBUSI1
SBUSI0
SBUS03
SBUS02
SBUS01
SBUS00
BUSRQ
SEL2L
K4
74LS175
S20LS
RGTR
BYTE3
BYTE3
BYTE2
BYTE2
BYTE1
BYTE1
BYTE0
BYTE0
8JHT
SUNELL COMPUTER DEVELOPMENT DIVISION
C
CODE IDENT 09132
DWG NO. 96870580
REV 01
SHEET 10



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8JHT					
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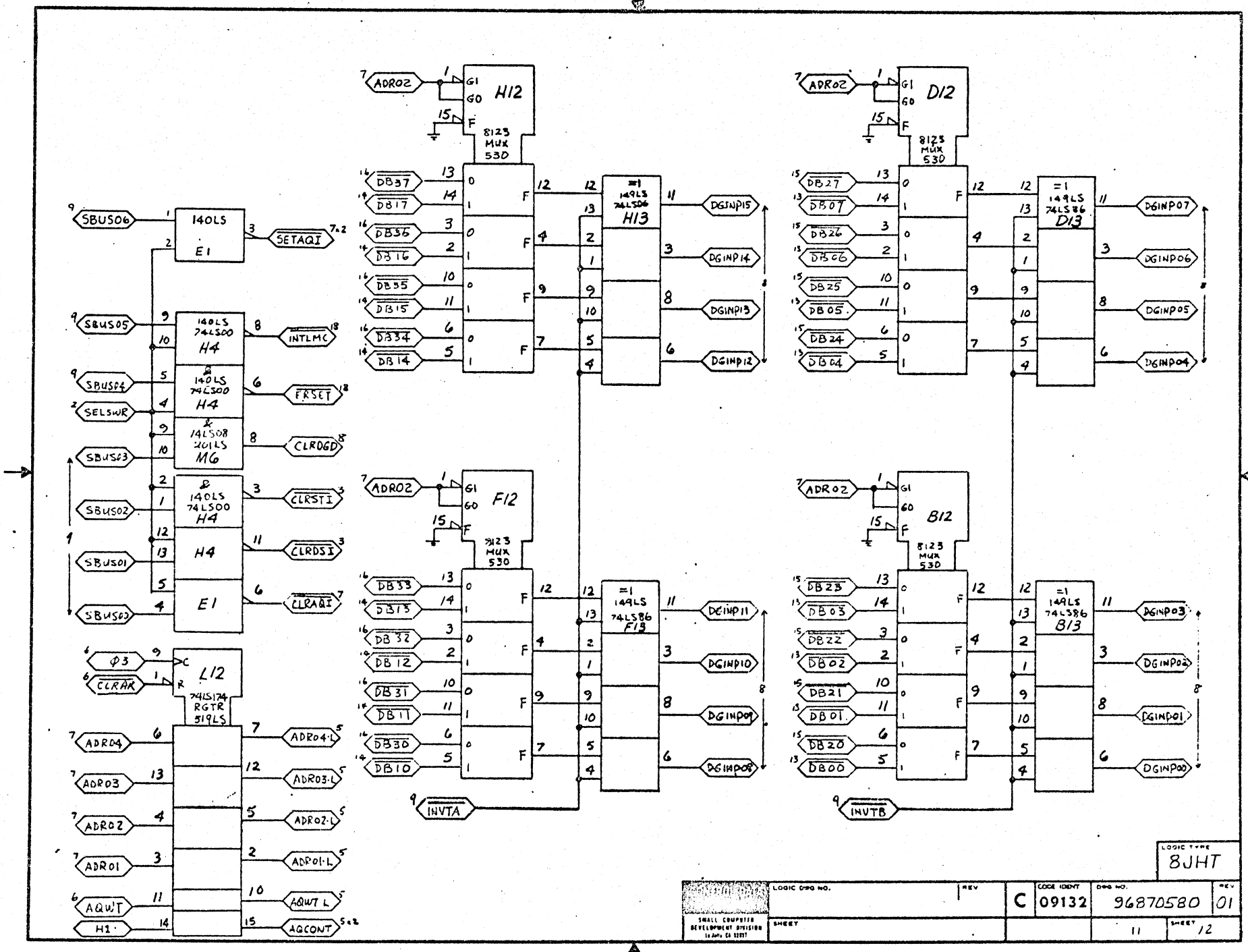
SURVEY				10	SHEET 11


SBUS06
140LS
E1
SETAQI
SBUS05
140LS 74LS00
H4
INTLMC
SBUS04
140LS 74LS00
H4
FRSET
SELSWR
14LS08 20LS
M6
SBUS03
CLRDGD
SBUS02
140LS 74LS00
H4
CLRSTI
SBUS01
H4
CLRDSI
SBUS03
E1
CLRAQI
Φ3
CLRAR
L12
74LS174 RGTR 519LS
ADR04
ADR03
ADR02
ADR01
AQWT
H1
ADR04-L
ADR03-L
ADR02-L
ADR01-L
AQWT L
AQCONT
ADR02
H12
8123 MUX 530
DB37
DB17
DB36
DB16
DB35
DB15
DB34
DB14
=1 14LS 74LS86
H13
DGINP15
DGINP14
DGINP13
DGINP12
F12
DB33
DB13
DB32
DB12
DB31
DB11
DB30
DB10
F13
DGINP11
DGINP10
DGINP09
DGINP08
INVTA
D12
DB27
DB07
DB26
DB06
DB25
DB05
DB24
DB04
D13
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DGINP06
DGINP05
DGINP04
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DB02
DB21
DB01
DB20
DB00
B13
DGINP03
DGINP02
DGINP01
DGINP00
INVTB
LOGIC TYPE
8JHT
LOGIC DWG NO.
REV
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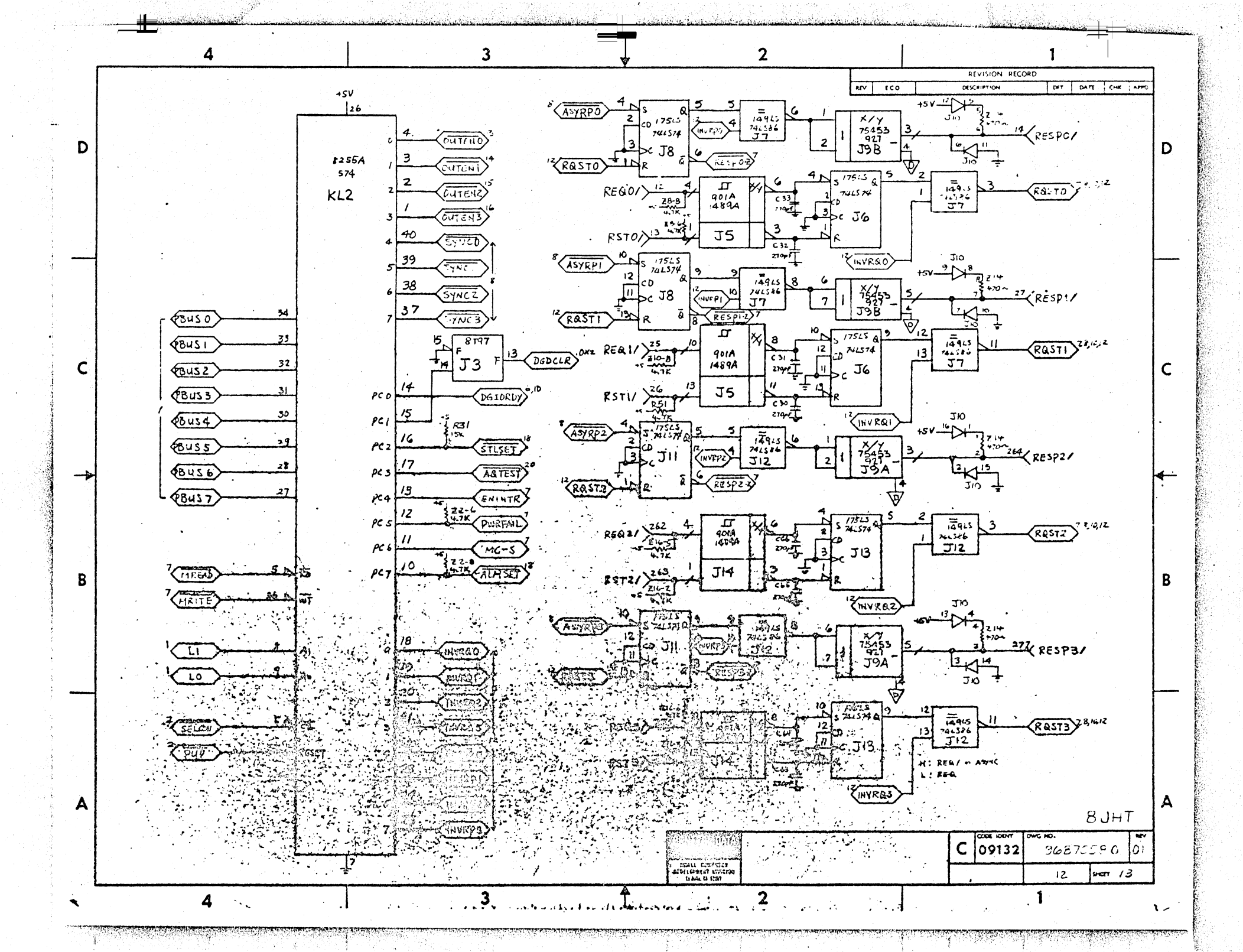
DWG NO.
96870580
REV
01
SMALL COMPUTER DEVELOPMENT DIVISION
SHEET
11
SHEET 12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574
KL2
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OUTEN1
OUTEN2
OUTEN3
SYNC0
SYNC
SYNC2
SYNC3
PBUS0
PBUS1
PBUS2
PBUS3
PBUS4
PBUS5
PBUS6
PBUS7
8T97
J3
DGDCLR
DGIORDY
PC0
PC1
PC2
PC3
PC4
PC5
PC6
PC7
R31
STLSET
A&TEST
ENINTR
PWRFAIL
MG-S
ALMSET
MREAD
MRITE
LI
LO
SELCH
SWP
INVRQ0
INVRQ1
INVRQ2
INVRQ3
INVRP4
ASYRP0
RQST0
REQ0/
RST0/
J8
J5
J6
J7
J9B
J10
RESP0/
RQST0
ASYRP1
RQST1
REQ1/
RST1/
RESP1/
ASYRP2
RQST2
J11
J12
J9A
RESP2/
REQ2/
RST2/
J13
J14
RESP3/
ASYRP3
RQST3
J18
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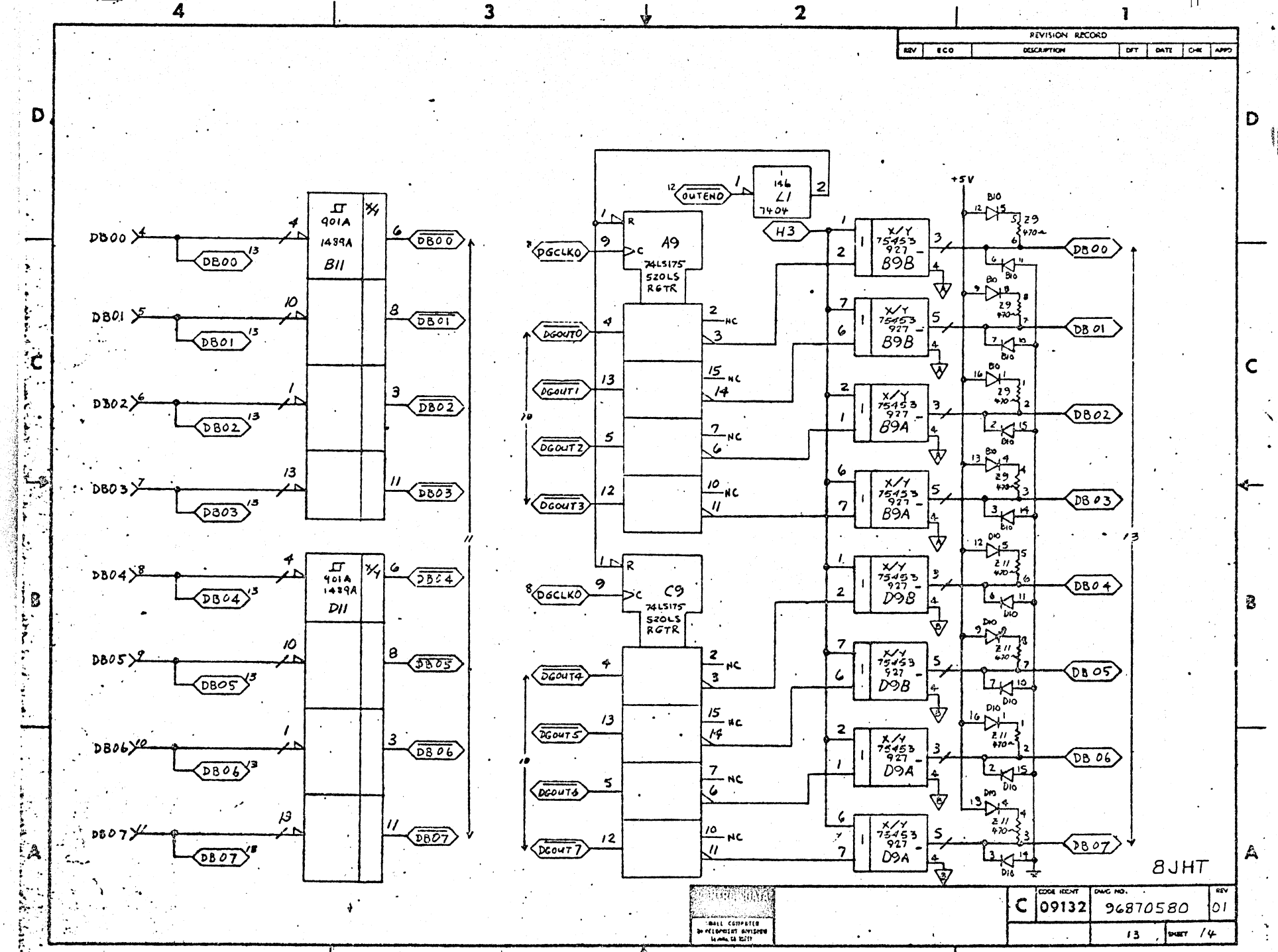
L: REQ
8JHT
C
09132
DWG NO.
REV
01
SHEET 13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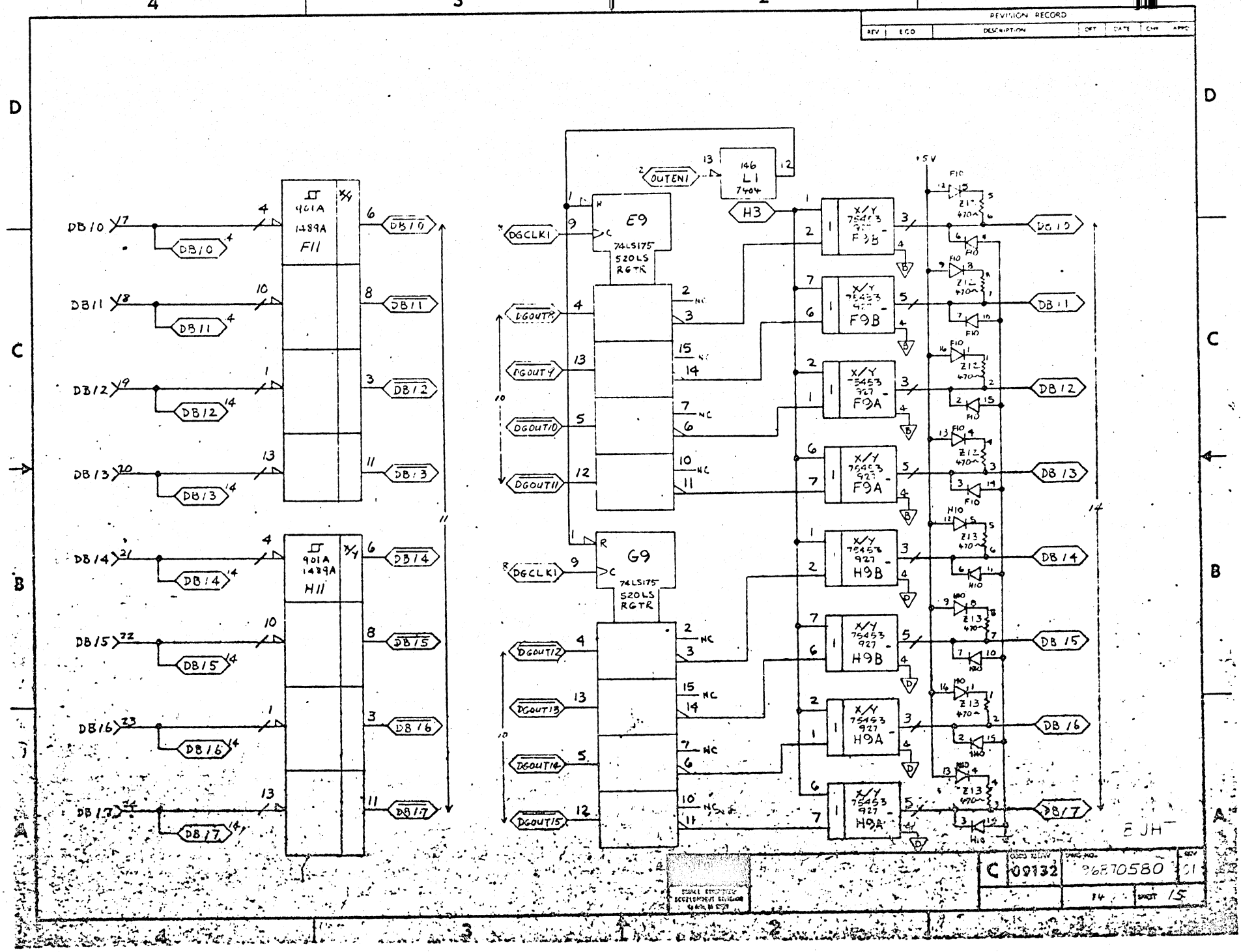
DB02
DB03
DB04
DB05
DB06
DB07
901A 1489A B11
901A 1489A D11
OUTENO
H3
DGCLKO
DGOUT0
DGOUT1
DGOUT2
DGOUT3
DGOUT4
DGOUT5
DGOUT6
DGOUT7
A9
C9
74LS175 S20LS RGTR
+5V
X/Y 75453 927 - B9B
X/Y 75453 927 - B9A
X/Y 75453 927 - D9B
X/Y 75453 927 - D9A
8JHT
BALL COMPUTER
C
09132
96870580
01
13
SHEET 14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DB11
DB12
DB13
DB14
DB15
DB16
DB17
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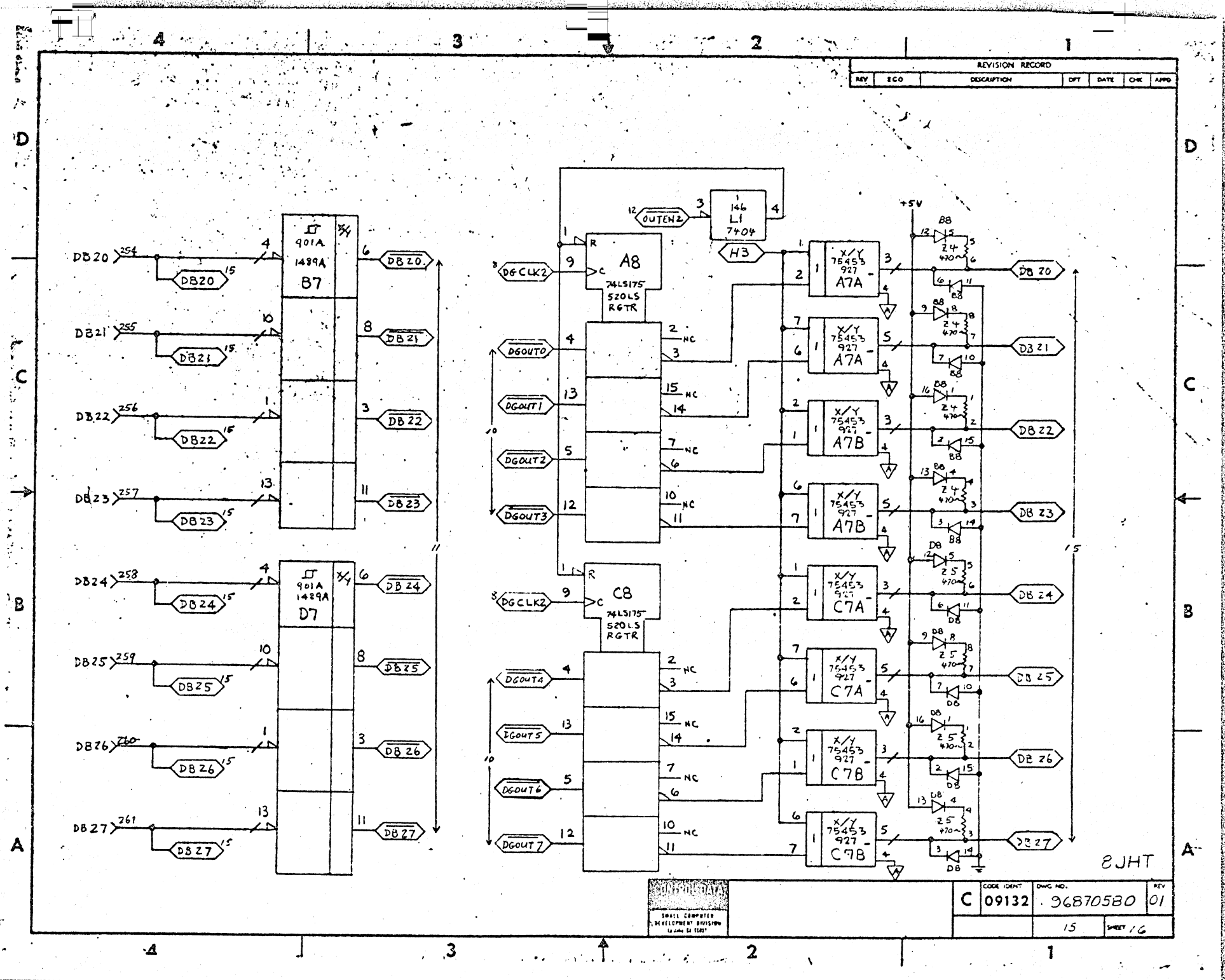
901A 1489A H11
OUTEN1
146 L1 7404
E9
G9
74LS175 S20LS RGTR
DGCLK1
DGOUT4
DGOUT7
DGOUT10
DGOUT11
DGOUT12
DGOUT13
DGOUT15
H3
X/Y 75453 927 F9B
X/Y 75453 927 F9A
X/Y 75453 927 H9B
X/Y 75453 927 H9A
+5V
Z10 470Ω
Z11 470Ω
Z12 470Ω
Z13 470Ω
F10
H10
8 JH
C
09132
96870580
01
14
SHEET 15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APPD
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DB21
DB22
DB23
DB24
DB25
DB26
DB27
901A 1489A B7
901A 1489A D7
A8
C8
74LS175 520LS RGTR
DGCLK2
DGOUT0
DGOUT1
DGOUT2
DGOUT3
DGOUT4
DGOUT5
DGOUT6
DGOUT7
OUTEN2
H3
+5V
X/Y 75453 927 A7A
X/Y 75453 927 A7B
X/Y 75453 927 C7A
X/Y 75453 927 C7B
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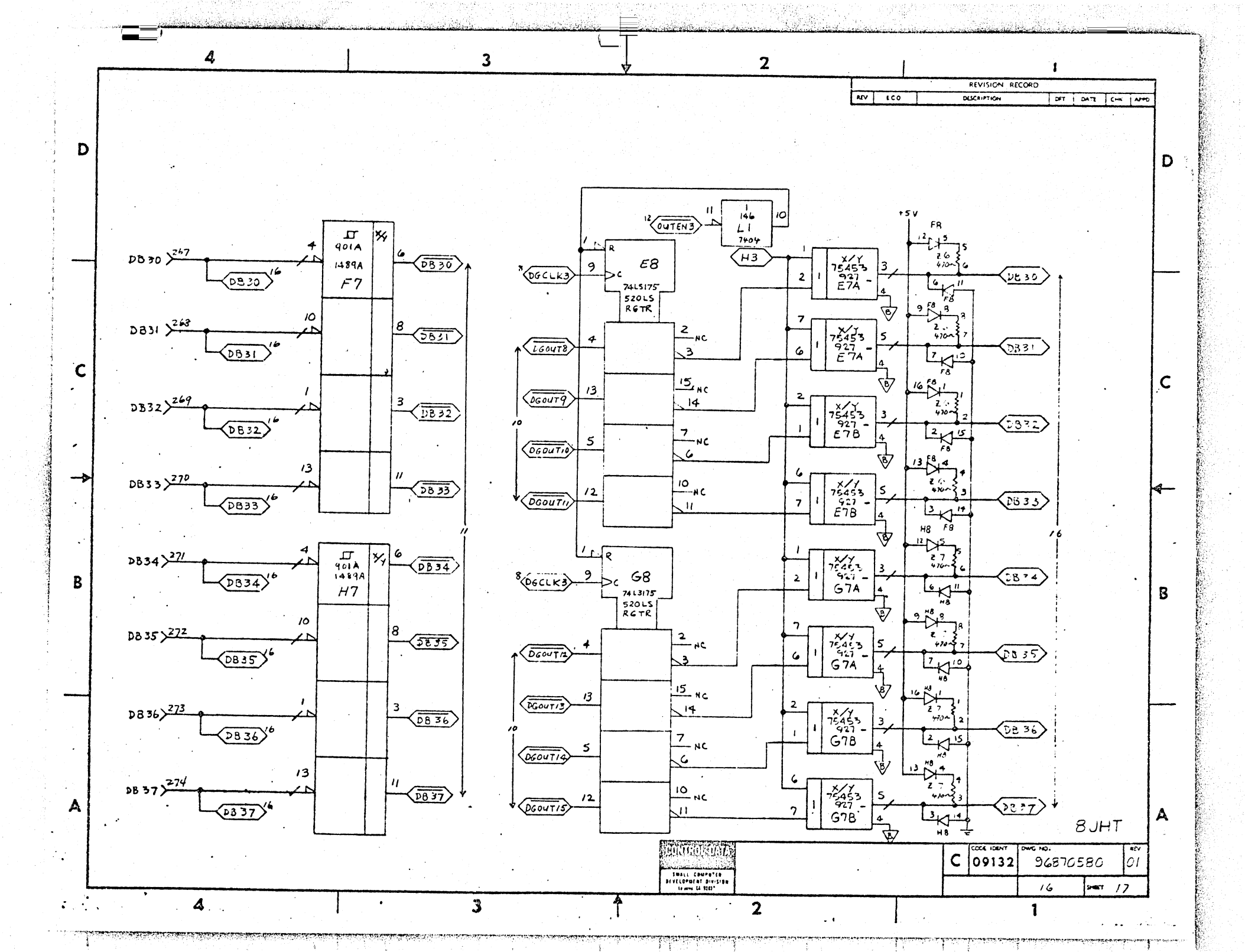
Z5 470
8JHT
SMALL COMPUTER DEVELOPMENT DIVISION
C
09132
96870580
01
15
SHEET 16


REVISION RECORD
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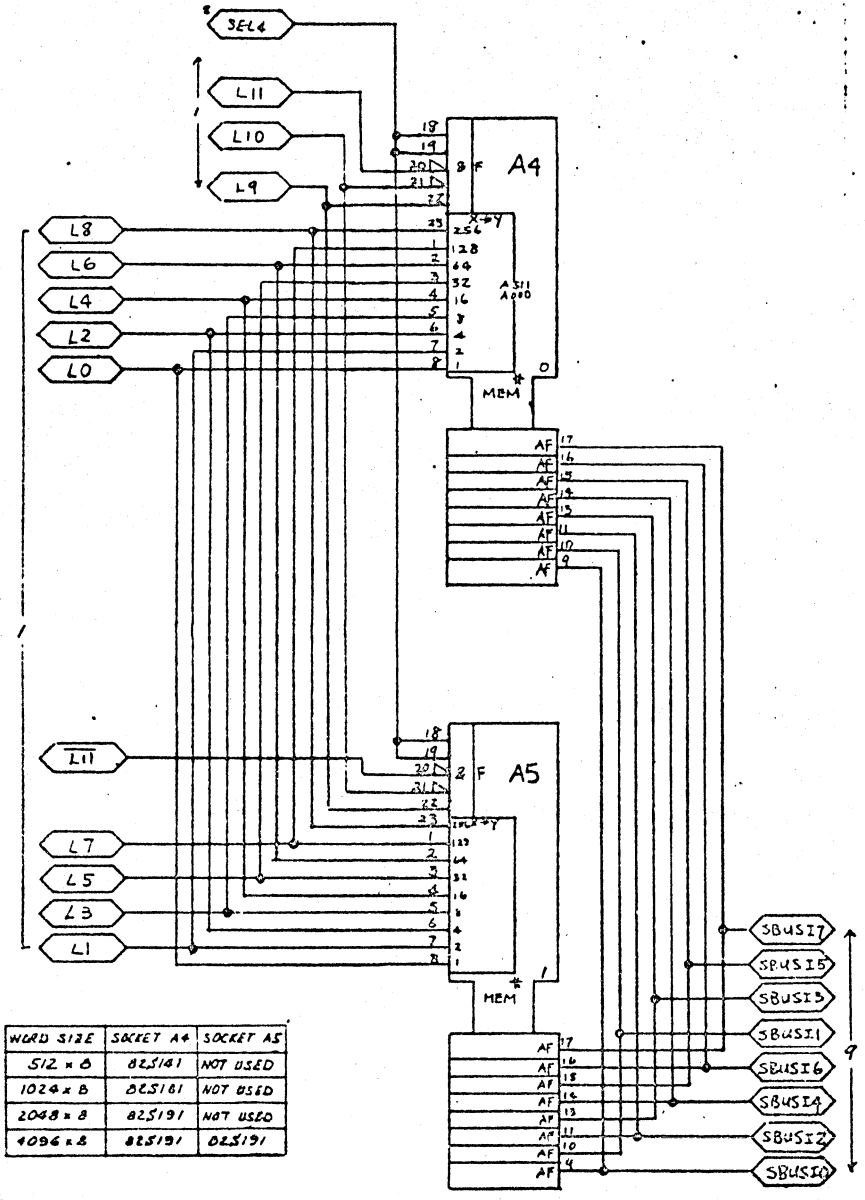
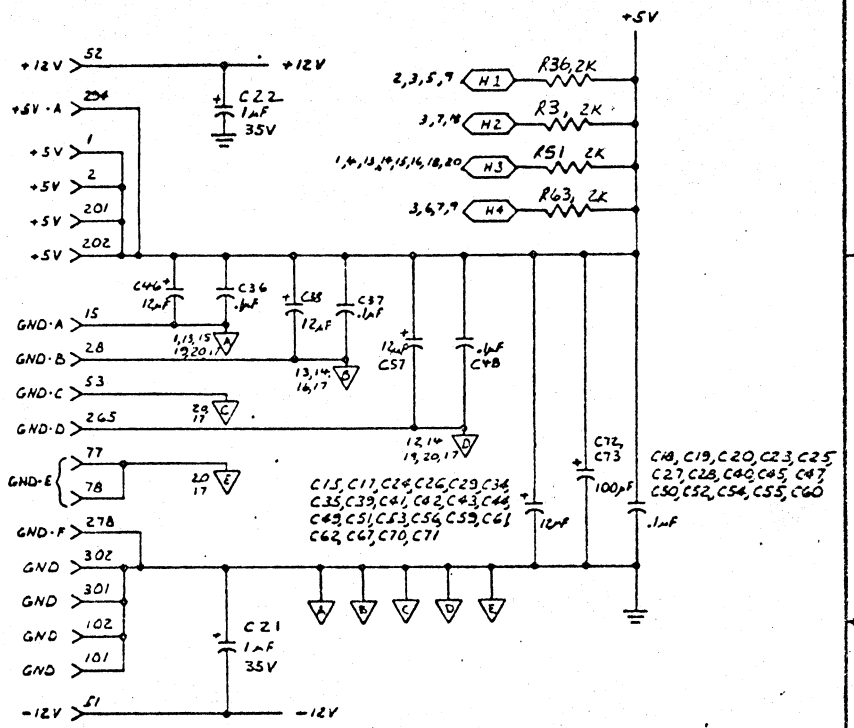
DB31 268
DB32 269
DB33 270
DB34 271
DB35 272
DB36 273
DB37 274
901A 1489A F7
901A 1489A H7
OUTEN3
DGCLK3
LGOUT8
DGOUT9
DGOUT10
DGOUT11
DGOUT12
DGOUT13
DGOUT14
DGOUT15
74LS175 520LS RGTR
E8
G8
H3
+5V
FB
H8
X/Y 75453 927 E7A
X/Y 75453 927 E7B
X/Y 75453 927 G7A
X/Y 75453 927 G7B
8JHT
SMALL COMPUTER DEVELOPMENT DIVISION
C 09132 96870580 01
16 SHEET 17

REVISION RECORD						
REV	ECO	DESCRIPTION	DFT	DATE	CHK	APPD

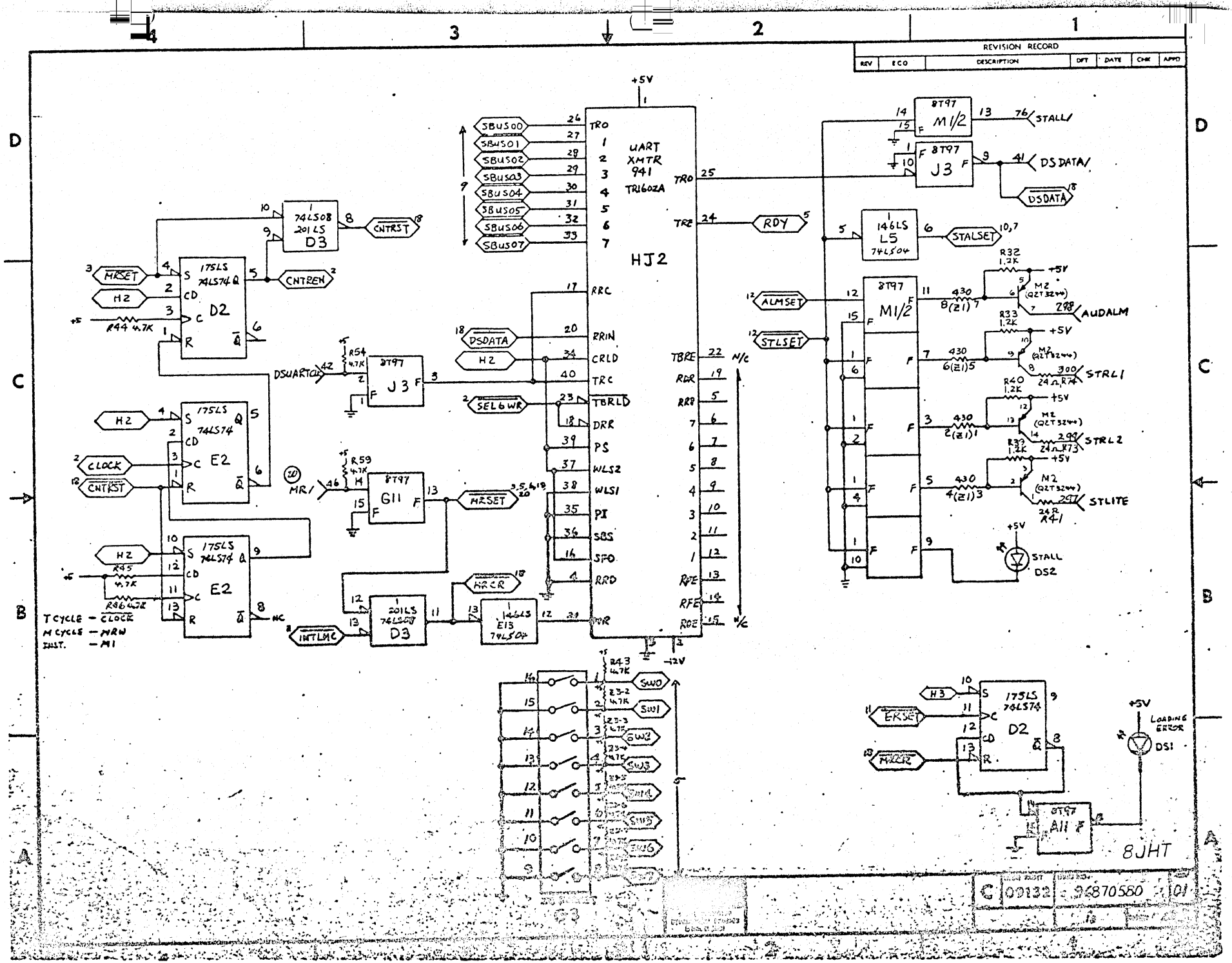


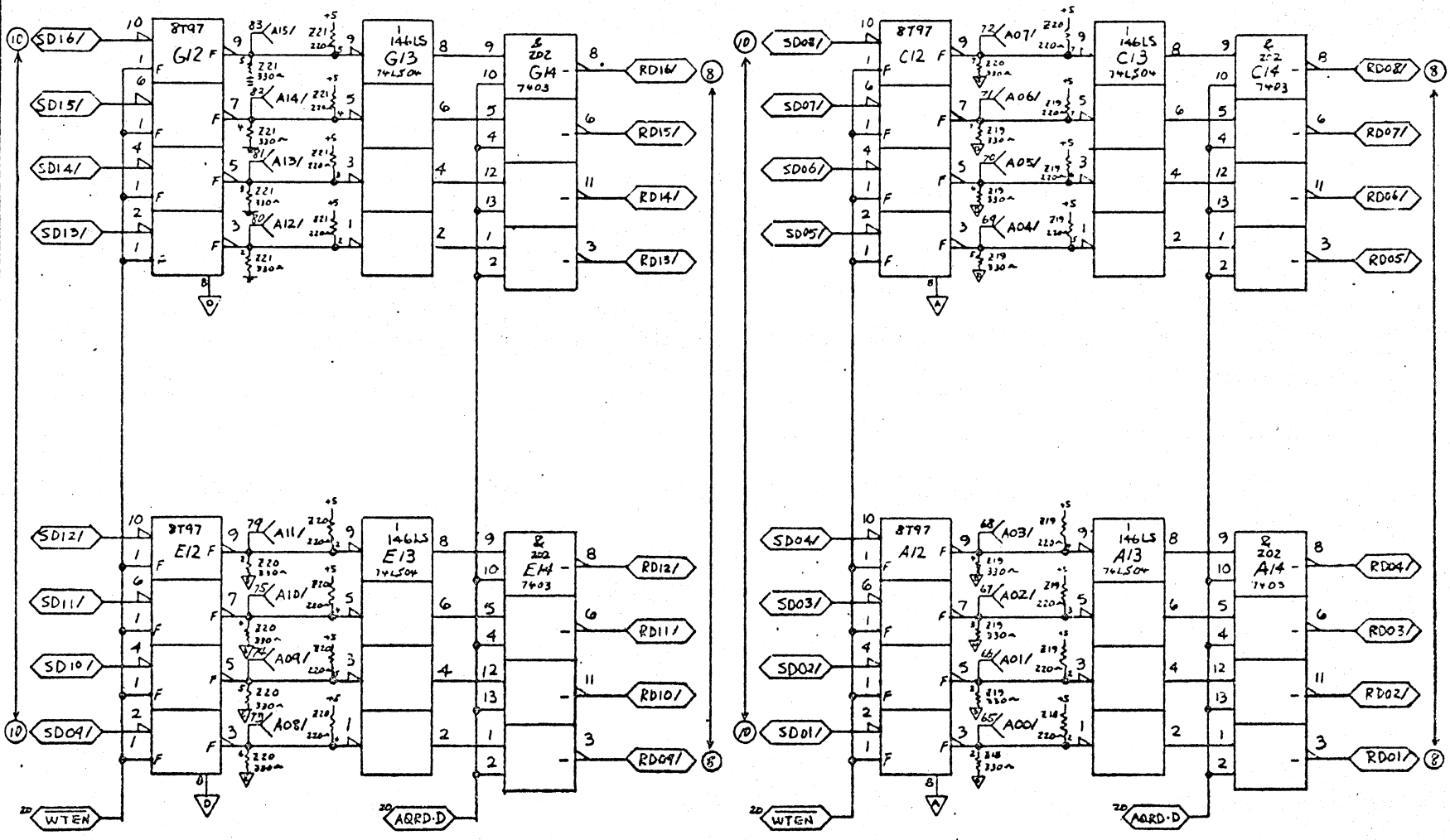
WORD SIZE	SOCKET A4	SOCKET A5
512 x 8	825141	NOT USED
1024 x 8	825161	NOT USED
2048 x 8	825191	NOT USED
4096 x 8	825191	825191

INSTEAD OF ACTUAL IC(S)
* DENOTES THAT 24 PIN DIP IC SOCKETS WILL BE INSTALLED



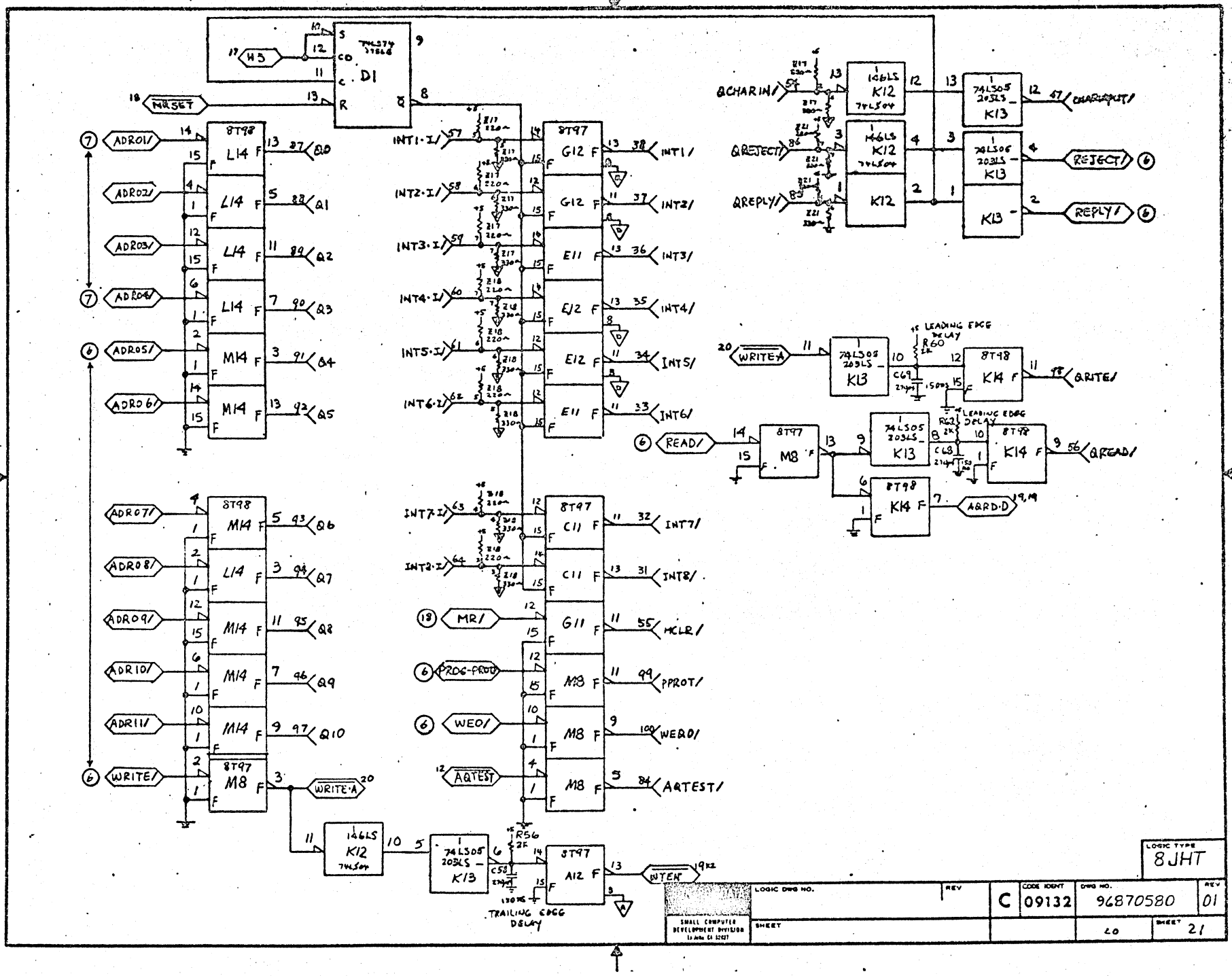
SMALL COMPUTER DEVELOPMENT DIVISION		C	CODE IDENT 09132	DWG NO. 96		REV 01
				17	SHEET 18	


REVISION RECORD
REV
ECO
DESCRIPTION
DFT
DATE
CHK
APPD
HJ2
UART XMTR 941 TRI602A
+5V
-12V
SBUS00
SBUS01
SBUS02
SBUS03
SBUS04
SBUS05
SBUS06
SBUS07
TRO
TRE
RRC
RRIN
CRLD
TRC
TBRLD
DRR
PS
WLS2
WLS1
PI
SBS
SFO
RRD
TBRE
RDR
RRB
RFE
RFE
RDE
RDY
DSDATA
H2
SEL6WR
MRSET
MR/
MRCR
INTLMC
CNTRST
CNTREN
DSUARTCLK
CLOCK
H3
ERSET
MRCLR
STALL/
DSDATA/
DSDATA
STALSET
ALMSET
STLSET
AUDALM
STRL1
STRL2
STLITE
STALL
DS2
LOADING ERROR
DS1
SW0
SW1
SW2
SW3
SW4
SW5
SW6
SW7
T CYCLE – CLOCK
M CYCLE – MRW
INST. – M1
8JHT
C
00132
96870580
101



LOGIC TYPE 8 JHT

LOGIC DWG NO.	REV	CODE IDENT	DWG NO.	REV
	C	09132	96870580	01
SHEET			19	SHEET 20


D1
MRSET
MS
ADR01/
ADR02/
ADR03/
ADR04/
ADR05/
ADR06/
ADR07/
ADR08/
ADR09/
ADR10/
ADR11/
WRITE/
INT1·I/
INT2·I/
INT3·I/
INT4·I/
INT5·I/
INT6·I/
INT7·I/
INT8·I/
MR/
PROC-PROT
WEO/
AQTEST
READ/
WRITE·A
WTEN
TRAILING EDGE DELAY
LEADING EDGE DELAY
BCHARIN/
QREJECT/
QREPLY/
CHARACKOUT/
REJECT/
REPLY/
WRITE/
QREAD/
AQRD·D
INT1/
INT2/
INT3/
INT4/
INT5/
INT6/
INT7/
INT8/
HCLR/
PPROT/
WEROI/
AQTEST/
LOGIC TYPE 8JHT
LOGIC DWG NO.
REV
C
CODE IDENT 09132
DWG NO. 96870580
REV 01
SHEET 21
SMALL COMPUTER DEVELOPMENT DIVISION

REV.	DATE	INITIAL

PIN	Comp Rec PAGE	PROPOSITION NAME
1	17	+5V
2	17	+5V
3		
4	13	DB00
5	13	DB01
6	13	DB02
7	13	DB03
8	13	DB04
9	13	DB05
10	13	DB06
11	13	DB07
12	12	FERC/
13	12	RSTQ/
14	12	RESPC/
15	17	GND-A
16		
17	14	DB10
18	14	DB11
19	14	DB12
20	14	DB13
21	14	DB14
22	14	DB15
23	14	DB16
24	14	DB17
25	12	REQI/
26	12	RSTI/
27	12	RESPI/
28	17	GND-B
29		
30		
31	20	INT8/
32	20	INT7/
33	20	INT6/
34	20	INT5/
35	20	INT4/
36	20	INT3/
37	20	INT2/
38	20	INT1/
39	7	INTERRUPT/
40		
41	18	DSDATA/
42	18	DSUARTCLK
43	3	DSTTL/
44	3	SM204/
45	3	DSCC/
46	3,20	MR/
47	7,20	CHARINPUT/
48		
49		
50		
51	17	-12V

PIN	Comp Rec PAGE	PROPOSITION NAME
52	17	+12V
53	17	GND-C
54	20	QCHARIN/
55	20	MCLR/
56	20	QREAD/
57	20	INT1 I/
58	20	INT2 I/
59	20	INT3 I/
60	20	INT4 I/
61	20	INT5 I/
62	20	INT6 I/
63	20	INT7 I/
64	20	INT8 I/
65	19	A00/
66	19	A01/
67	19	A02/
68	19	A03/
69	19	A04/
70	19	A05/
71	19	A06/
72	19	A07/
73	19	A08/
74	19	A09/
75	19	A10/
76	18	STALL/
77	17	GND-E
78	17	GND-E
79	19	A11/
80	19	A12/
81	19	A13/
82	19	A14/
83	19	A15/
84	20	QTEST/
85	20	QREPLY/
86	20	QREJECT/
87	20	Q0
88	20	Q1
89	20	Q2
90	20	Q3
91	20	Q4
92	20	Q5
93	20	Q6
94	20	Q7
95	20	Q8
96	20	Q9
97	20	Q10
98	20	QRITE/
99	20	PPROT/
100	20	WEQ0/
101	17	GND
102	17	GND

PIN	Comp Rec PAGE	PROPOSITION NAME
201	17	+5V
202	17	+5V
203	10,19	SD01/
204	8,19	RD01/
205	10,19	SD02/
206	8,19	RD02/
207	10,19	SD03/
208	8,19	RD03/
209	10,19	SD04/
210	8,19	RD04/
211	10,19	SD05/
212	6,20	ADR05/
213		
214	8,19	RD05/
215	10,19	SD06/
216	6,20	REPLY/
217	6,20	ADR06/
218	8,19	RD06/
219	10,19	SD07/
220	6,20	REJECT/
221	8,19	RD07/
222	6,20	ADR07/
223	10,19	SD08/
224	8,19	RD08/
225	10,19	SD09/
226	8,19	RD09/
227		
228	10,19	SD10/
229	8,19	RD10/
230	10,19	SD11/
231	8,19	RD11/
232		
233	10,19	SD12/
234	8,19	RD12/
235	10,19	SD13/
236	8,19	RD13/
237		
238	10,19	SD14/
239	8,19	RD14/
240	10,19	SD15/
241	8,19	RD15/
242	7	POWFAIL/
243	10,19	SD16/
244	8,19	RD16/
245	7,20	ADR04/
246	7,20	ADR03/
247	7,20	ADR02/
248	6,20	READ/
249		
250		
251	3	ACFAIL/

PIN	Comp Rec PAGE	PROPOSITION NAME
252		
253		
254	15	DB20
255	15	DB21
256	15	DB22
257	15	DB23
258	15	DB24
259	15	DB25
260	15	DB26
261	15	DB27
262	12	REQ2/
263	12	RST2/
264	12	RESP2/
265	17	GND-D
266		
267	16	DB30
268	16	DB31
269	16	DB32
270	16	DB33
271	16	DB34
272	16	DB35
273	16	DB36
274	16	DB37
275	12	REQ3/
276	12	RST3/
277	12	RESP3/
278	17	GND-F
279	3	STLOFF/
280	7,20	ADR01/
281	6,20	ADR08/
282	6,20	ADR09/
283	6,20	ADR10/
284	6,20	ADR11/
285		(ADR12/)
286		(ADR13/)
287		(ADR14/)
288		(ADR15/)
289		(ADR16/)
290	6,20	WRITE/
291	6,20	PROG-PROT/
292	6,20	WEO/
293	7	MC-S/
294	17	+5V-A
295	3	FLDSTL/
296	3	RESET/
297	18	STLITE
298	18	AUDALM
299	18	STRLR
300	18	STRL1
301	17	GND
302	17	GND

8JHT

REV 01

96870580

REV.	DATE	INITIAL
-1	1-25-8	AW
01	5-4-8	AW
02	6-29-8	AW

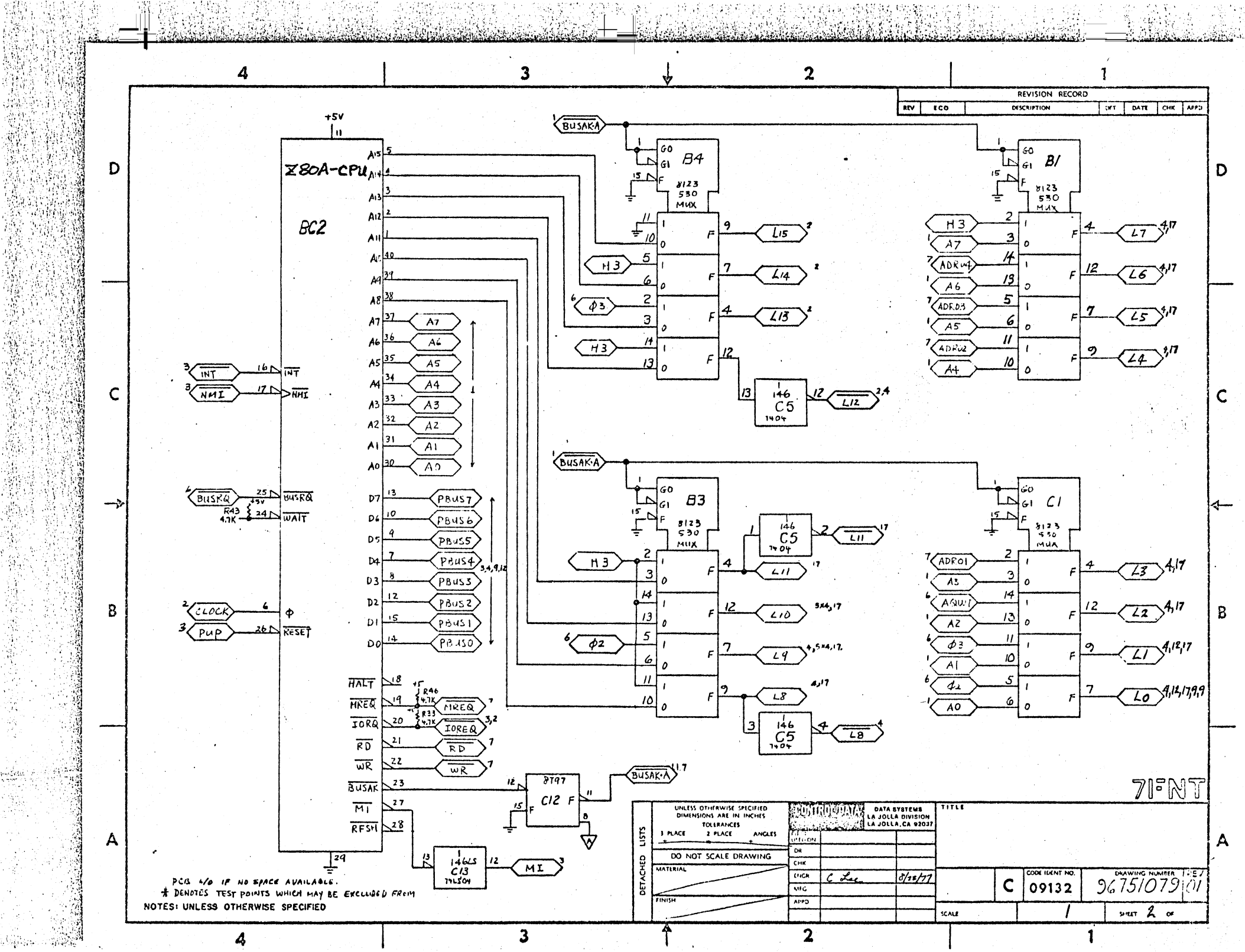
PIN	Cross Ref PAGE	PROPOSITION NAME
1	17	+5V
2	17	+5V
3		
4	13	DB00
5	13	DB01
6	13	DB02
7	13	DB03
8	13	DB04
9	13	DB05
10	13	DB06
11	13	DB07
12	12	REQ0/
13	12	RST0/
14	12	RESP0/
15	17	GND-A
16		
17	14	DB10
18	14	DB11
19	14	DB12
20	14	DB13
21	14	DB14
22	14	DB15
23	14	DB16
24	14	DB17
25	12	REQ1/
26	12	RST1/
27	12	RESP1/
28	17	GND-B
29		
30		
31	20	INT8/
32	20	INT7/
33	20	INT6/
34	20	INT5/
35	20	INT4/
36	20	INT3/
37	20	INT2/
38	20	INT1/
39	7	INTERRUPT/
40		
41	18	DSDATA/
42	18	DSUARTCLK
43	3	DSTTL/
44	3	SM204/
45	3	DSCC/
46	3,20	MR/
47	7,20	CHARINPUT/
48		
49		
50		
51	17	-12V

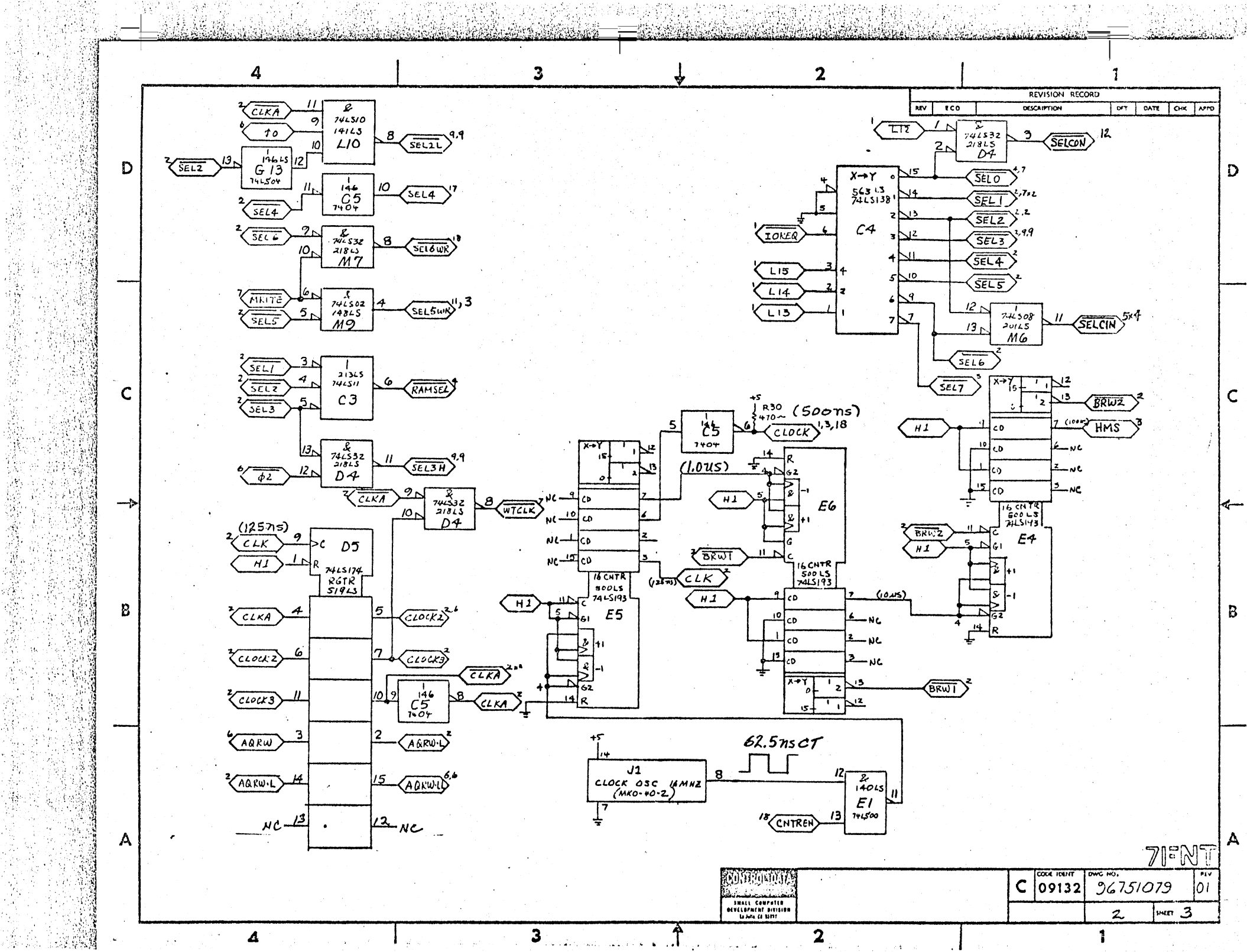
PIN	Cross Ref PAGE	PROPOSITION NAME
52	17	+12V
53	17	GND-C
54	20	QCHARIN/
55	20	MCLR/
56	20	QREAD/
57	20	INT1·I/
58	20	INT2·I/
59	20	INT3·I/
60	20	INT4·I/
61	20	INT5·I/
62	20	INT6·I/
63	20	INT7·I/
64	20	INT8·I/
65	19	A00/
66	19	A01/
67	19	A02/
68	19	A03/
69	19	A04/
70	19	A05/
71	19	A06/
72	19	A07/
73	19	A08/
74	19	A09/
75	19	A10/
76	18	STALL/
77	17	GND-E
78	17	GND-E
79	19	A11/
80	19	A12/
81	19	A13/
82	19	A14/
83	19	A15/
84	20	AQTEST/
85	20	QREPLY/
86	20	QREJECT/
87	20	Q0
88	20	Q1
89	20	Q2
90	20	Q3
91	20	Q4
92	20	Q5
93	20	Q6
94	20	Q7
95	20	Q8
96	20	Q9
97	20	Q10
98	20	QRITE/
99	20	PPROT/
100	20	WEQ0/
101	17	GND
102	17	GND

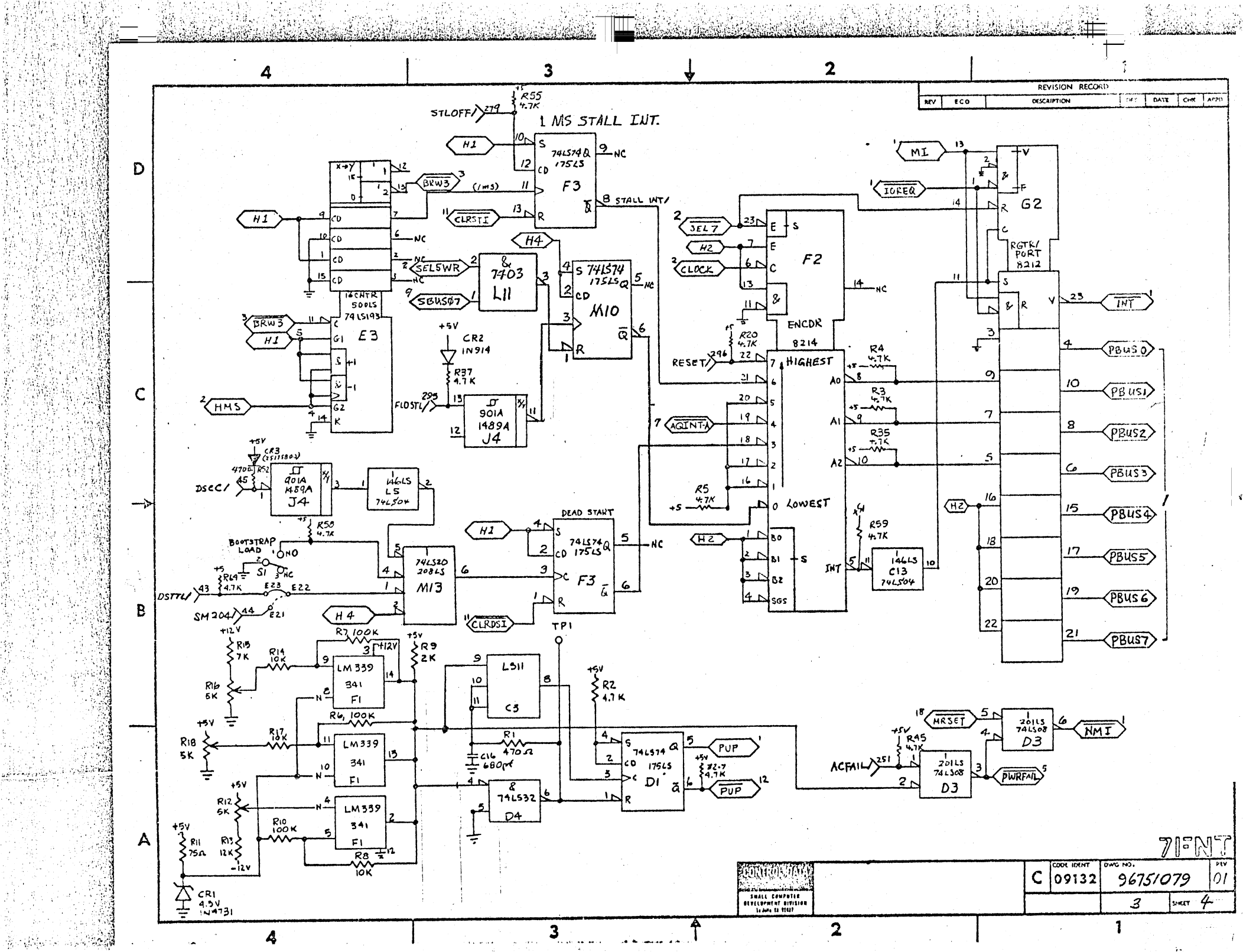
PIN	Cross Ref PAGE	PROPOSITION NAME
201	17	+5V
202	17	+5V
203	10,19	SD01/
204	8,19	RD01/
205	10,19	SD02/
206	8,19	RD02/
207	10,19	SD03/
208	8,19	RD03/
209	10,19	SD04/
210	8,19	RD04/
211	10,19	SD05/
212	6,20	ADR05/
213		RTERM/
214	8,19	RD05/
215	10,19	SD06/
216	6,20	REPLY/
217	6,20	ADR06/
218	8,19	RD06/
219	10,19	SD07/
220	6,20	REJECT/
221	8,19	RD07/
222	6,20	ADR07/
223	10,19	SD08/
224	8,19	RD08/
225	10,19	SD09/
226	8,19	RD09/
227		
228	10,19	SD10/
229	8,19	RD10/
230	10,19	SD11/
231	8,19	RD11/
232		
233	10,19	SD12/
234	8,19	RD12/
235	10,19	SD13/
236	8,19	RD13/
237		
238	10,19	SD14/
239	8,19	RD14/
240	10,19	SD15/
241	8,19	RD15/
242	7	POWFAIL/
243	10,19	SD16/
244	8,19	RD16/
245	7,20	ADR04/
246	7,20	ADR03/
247	7,20	ADR02/
248	6,20	READ/
249		
250		
251	3	ACFAIL/

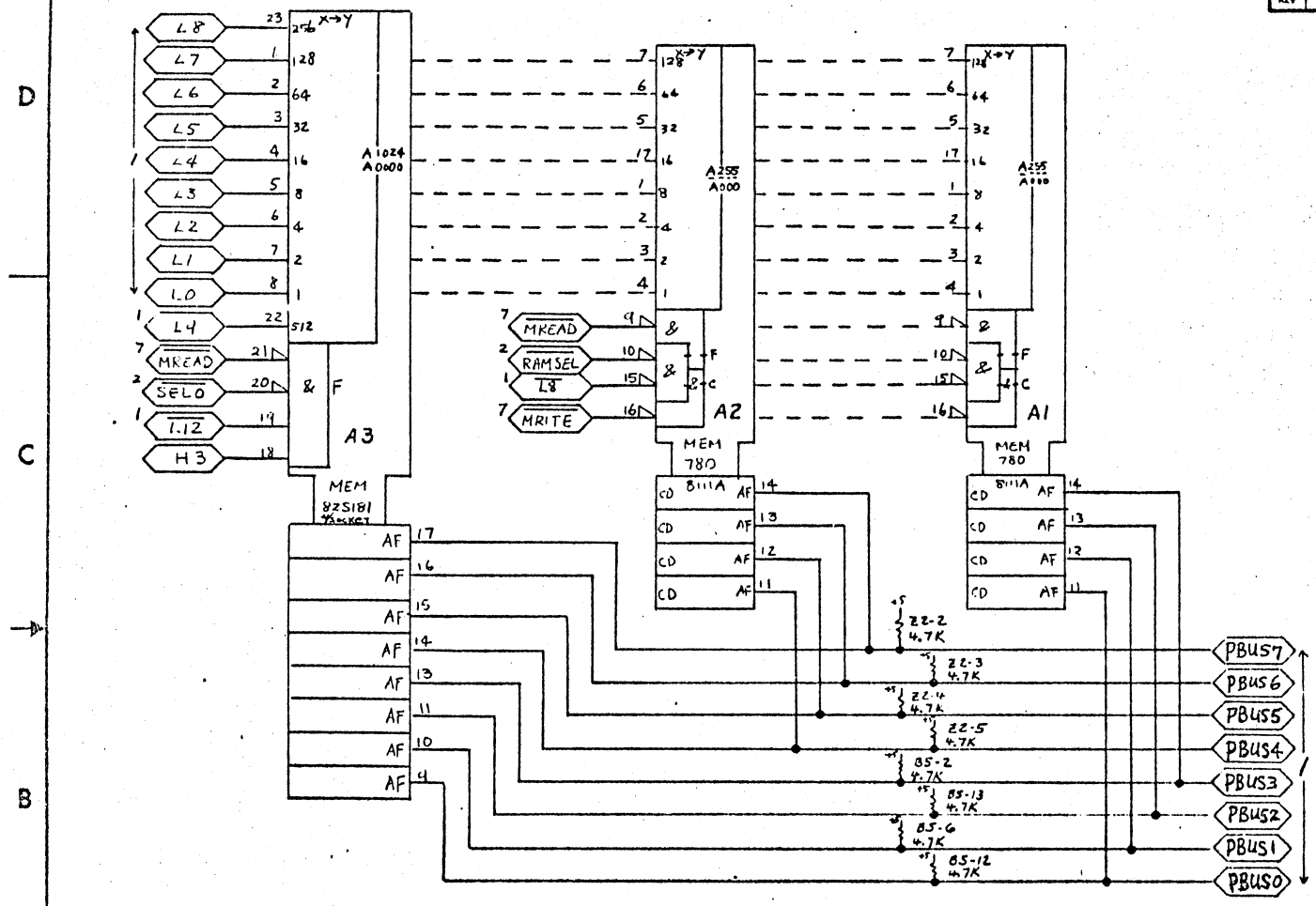
PIN	Cross Ref PAGE	PROPOSITION NAME
252		
253		
254	15	DB20
255	15	DB21
256	15	DB22
257	15	DB23
258	15	DB24
259	15	DB25
260	15	DB26
261	15	DB27
262	12	REQ2/
263	12	RST2/
264	12	RESP2/
265	17	GND-D
266		
267	16	DB30
268	16	DB31
269	16	DB32
270	16	DB33
271	16	DB34
272	16	DB35
273	16	DB36
274	16	DB37
275	12	REQ3/
276	12	RST3/
277	12	RESP3/
278	17	GND-F
279	3	STLOFF/
280	7,20	ADR01/
281	6,20	ADR08/
282	6,20	ADR09/
283	6,20	ADR10/
284	6,20	ADR11/
285		(ADR12/)
286		(ADR13/)
287		(ADR14/)
288		(ADR15/)
289		(ADR16/)
290	6,20	WRITE/
291	6,20	PROG-PROT/
292	6,20	WEQ/
293	7	MC-S/
294	17	+5V-A
295	3	FLDSTL/
296	3	RESET/
297	18	STLITE
298	18	AUDALM
299	18	STRL2
300	18	STRL1
301	17	GND
302	17	GND

71-INT
SH 1 OF 21


REVISION RECORD
REV
ECO
DESCRIPTION
DWT
DATE
CHK
APPD
Z80A-CPU
BC2
+5V
BUSAK·A
B4
B1
B3
C1
C5
8123 530 MUX
146 C5 7404
8T97 C12 F
146LS C13 74LS04
INT
NMI
BUSRQ
WAIT
CLOCK
PUP
RESET
HALT
MREQ
IOREQ
RD
WR
BUSAK
M1
RFSH
R46 4.7K
R33 4.7K
R43 4.7K
PBUS7
PBUS6
PBUS5
PBUS4
PBUS3
PBUS2
PBUS1
PBUS0
A7
A6
A5
A4
A3
A2
A1
A0
H3
Φ3
Φ2
ADR04
ADR03
ADR02
ADR01
AQUI
L15
L14
L13
L12
L11
L10
L9
L8
L7
L6
L5
L4
L3
L2
L1
L0
71-INT
DETACHED LISTS
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
3 PLACE
2 PLACE
ANGLES
DO NOT SCALE DRAWING
MATERIAL
FINISH
DATA SYSTEMS
LA JOLLA DIVISION
LA JOLLA, CA 92037
DR
CHK
ENGR
C Lee
8/22/77
MFG
APPD
TITLE
C
CODE IDENT NO.
09132
DRAWING NUMBER
96751079
REV
01
SCALE
1
SHEET 2 OF
PCB 4/0 IF NO SPACE AVAILABLE.
* DENOTES TEST POINTS WHICH MAY BE EXCLUDED FROM
NOTES: UNLESS OTHERWISE SPECIFIED


REVISION RECORD
REV | ECO | DESCRIPTION | DFT | DATE | CHK | APPD
CLKA
TO
SEL2
SEL4
SEL6
MRITE
SEL5
SEL1
SEL2
SEL3
Φ2
CLKA
CLK
H1
CLKA
CLOCK2
CLOCK3
AQRW
AQRW-L
NC
L10
G13
74LS04
C5
7404
M7
M9
C3
D4
D4
D5
74LS174
RGTR
519LS
SEL2L
SEL4
SEL6WR
SEL5WR
RAMSEL
SEL3H
WTCLK
CLOCK2
CLOCK3
CLKA
AQRW-L
AQRW-L
(125ns)
L12
SELCON
IOKER
L15
L14
L13
C4
X→Y
563 L3
74LS138
SEL0
SEL1
SEL2
SEL3
SEL4
SEL5
SEL6
SEL7
M6
SELCIN
5x4
R30
470Ω
(500ns)
CLOCK
1,3,18
(1.0µs)
E6
BRWT
BRWI
BRWZ
HMS
E4
E5
16 CNTR
500LS
74LS193
(10µs)
J1
CLOCK OSC 16MHZ
(MKO-40-2)
62.5nsCT
E1
74LS00
CNTREN
CONFIDENTIAL
SMALL COMPUTER DEVELOPMENT DIVISION
C
CODE IDENT 09132
DWG NO. 96751079
REV 01
SHEET 2 3
71 PINT


1 MS STALL INT.
REVISION RECORD
REV
ECO
DESCRIPTION
DATE
CHK
APPD
STLOFF/
R55 4.7K
H1
74LS74 Q 175LS F3
STALL INT/
BRW3
(1MS)
CLRSTI
H4
SEL5WR
SBUS07
7403 L11
74LS74 175LS Q M10
16 CNTR 500LS 74LS193 E3
BRW3
H1
HMS
CR2 IN914
R37 4.7K
FLOSTI/
901A 1489A J4
DSECI/
CR3 (SS1580A)
470Ω R52
74LS04 LS
BOOTSTRAP LOAD
NO
S1
NC
R49 4.7K
DSTTLI/
SM204/
74LS20 20LS M13
DEAD START
CLRDSI
TP1
R7 100K
+12V
R15 7K
R14 10K
R16 5K
LM339 341 F1
R9 2K
R6, 100K
R17 10K
R18 5K
R12 5K
R10 100K
R11 75Ω
R13 12K
-12V
R8 10K
CR1 4.3V 1N4731
L511 C3
R1 470Ω
C16 680pf
74LS32 D4
R2 4.7K
74LS74 175LS D1
PUP
PUP
#2-7 4.7K
MI
IOREQ
G2
RGTK/ PORT 8212
INT
PBUS0
PBUS1
PBUS2
PBUS3
PBUS4
PBUS5
PBUS6
PBUS7
SEL7
H2
CLOCK
F2
ENCDR 8214
RESET/
R20 4.7K
HIGHEST
LOWEST
AQINT-A
R5 4.7K
R4 4.7K
R3 4.7K
R35 4.7K
R59 4.7K
INT
14LS C13 74LS04
MRSET
20ILS 74LS08 D3
NMI
R45 4.7K
ACFAIL
PWRFAIL
71INT
SMALL COMPUTER DEVELOPMENT DIVISION
C
09132
DWG NO. 96751079
REV 01
SHEET 3 4



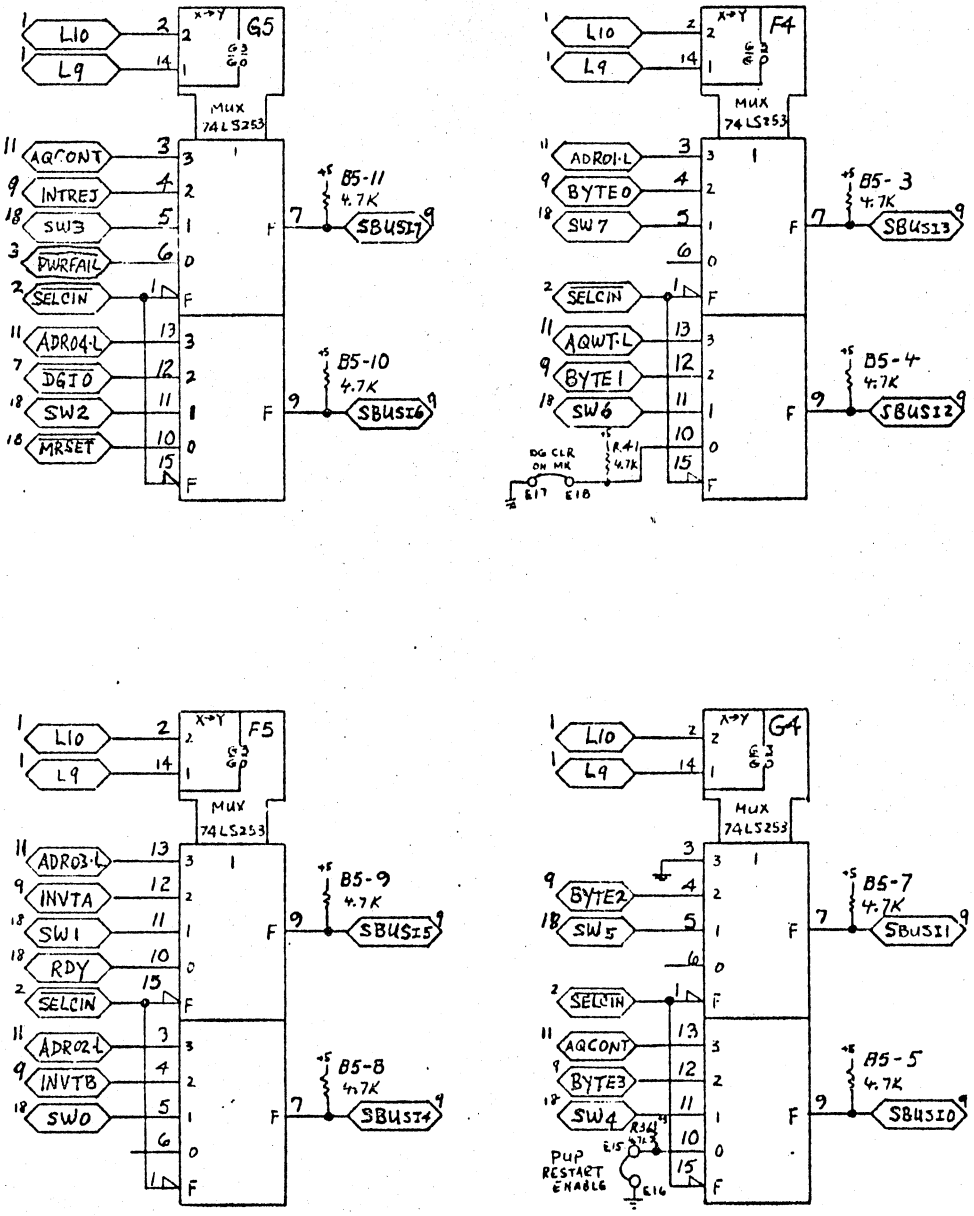
REVISION RECORD

REV	ECO	DESCRIPTION	DFT	DATE	CHK	APPD

71-NT

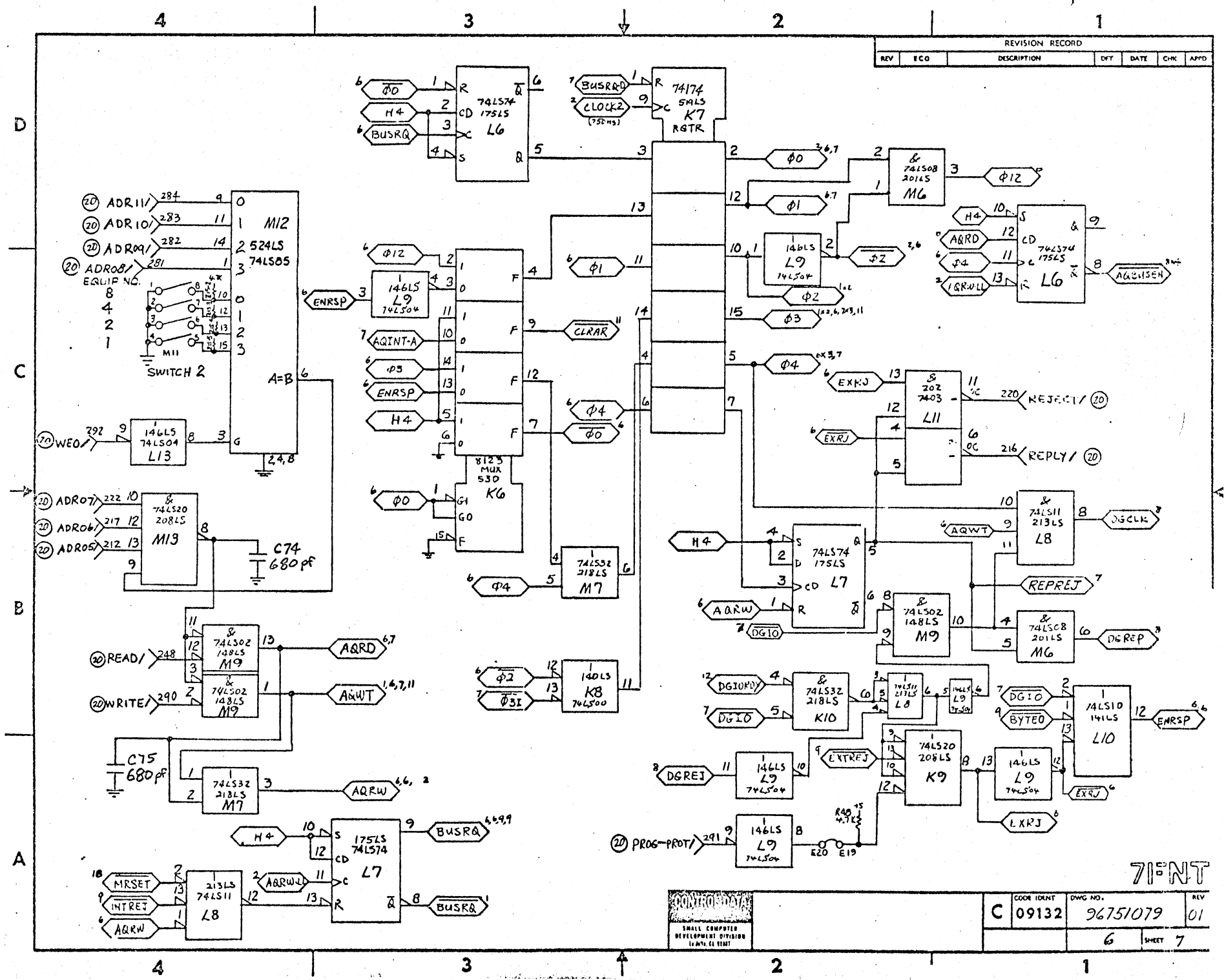
CONTROL DATA
SMALL COMPUTER DEVELOPMENT DIVISION

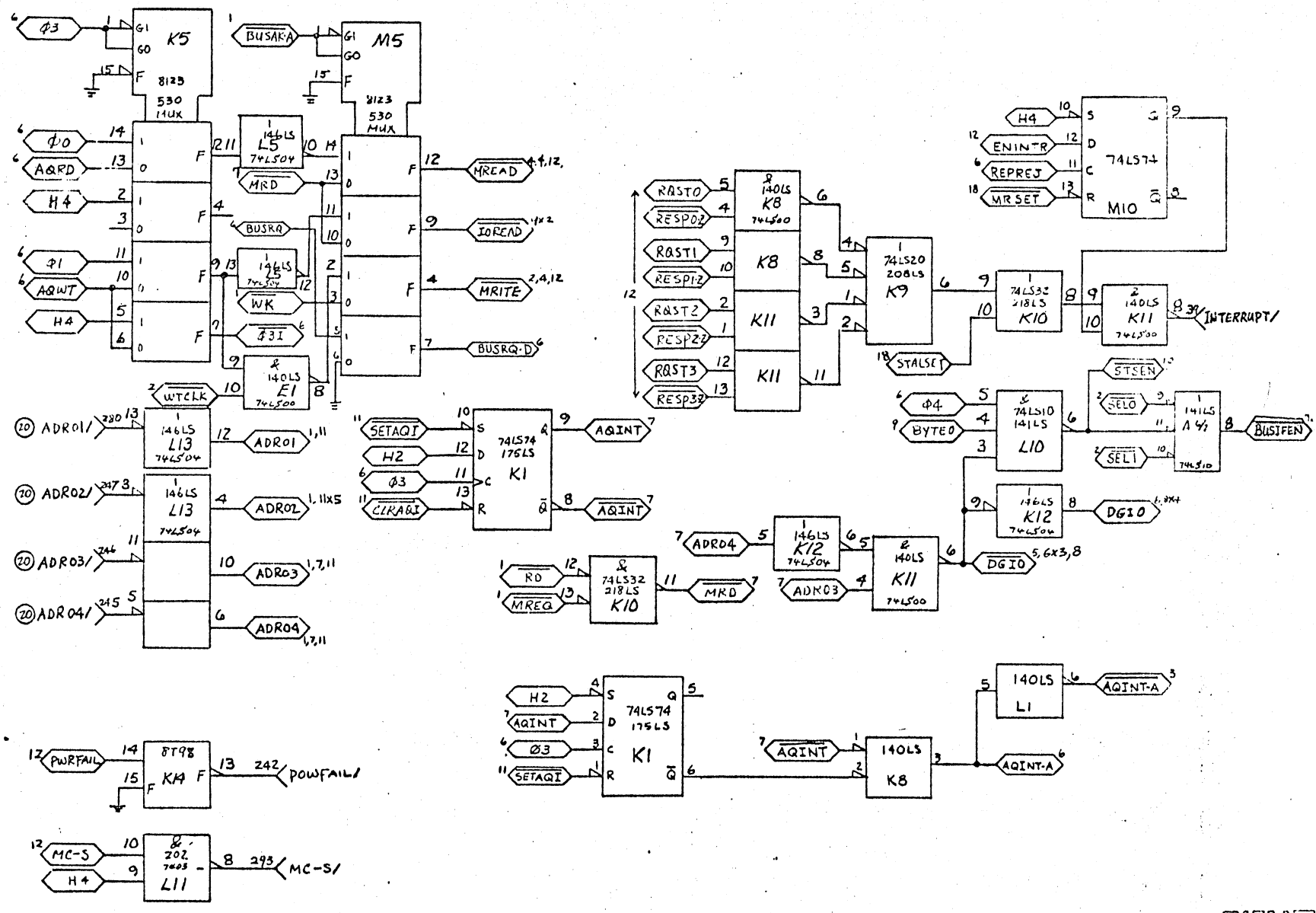
	CODE IDENT	DWG NO.	REV
C	09132	96751079	01
		4	SHEET 5

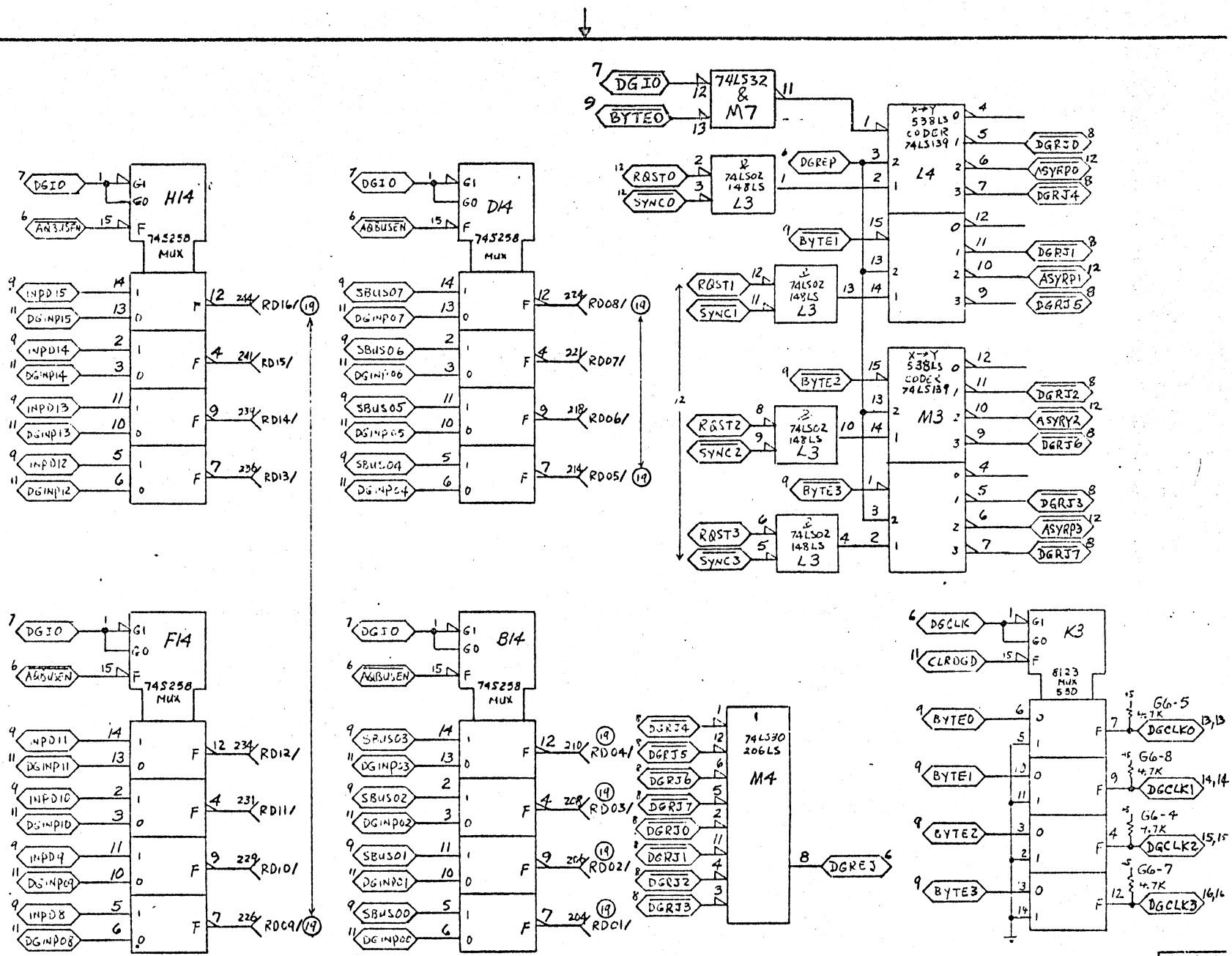


LOGIC TYPE 71-INT

CONTROL DATA SMALL COMPUTER DEVELOPMENT DIVISION	LOGIC DWG NO.	REV	C	CODE IDENT 09132	DWG NO. 96[illegible]079	REV 01
	SHEET				5	SHEET 6

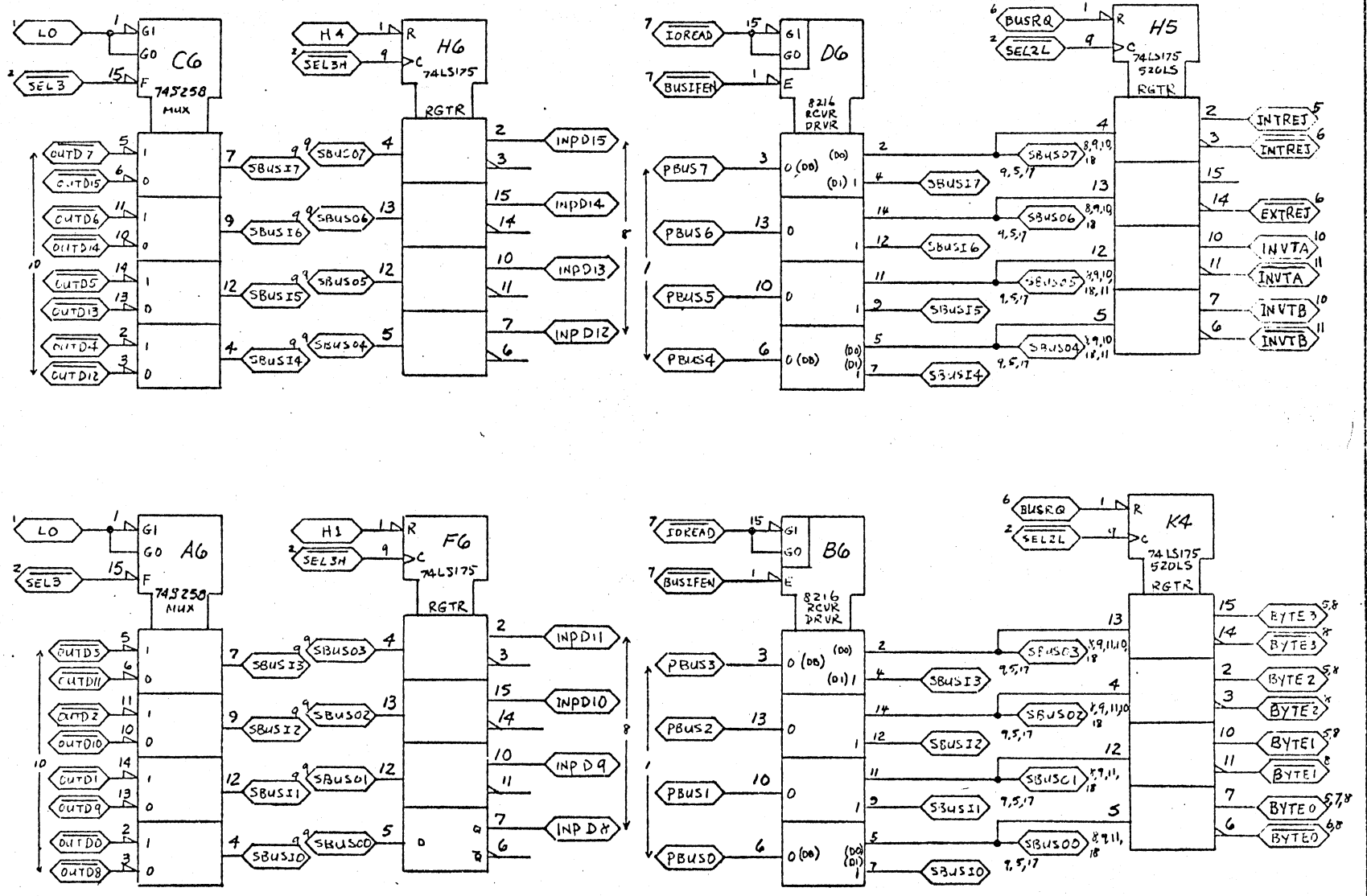

REVISION RECORD
REV | ECO | DESCRIPTION | DFT | DATE | CHK | APPD
74174 54LS K7 RGTR
74LS74 175LS L6
74LS74 175LS L7
74LS32 21BLS M7
74LS32 21BLS K8
74LS32 21BLS K10
74LS02 14BLS M9
74LS08 20LS M6
74LS20 20BLS M13
74LS20 20BLS K9
74LS11 21BLS L8
74LS10 14LS L10
74LS04 14LS L9
8123 MUX 53D K6
SWITCH 2
SMALL COMPUTER DEVELOPMENT DIVISION
CODE IDENT 09132
DWG NO. 967751079
REV 01
SHEET 7

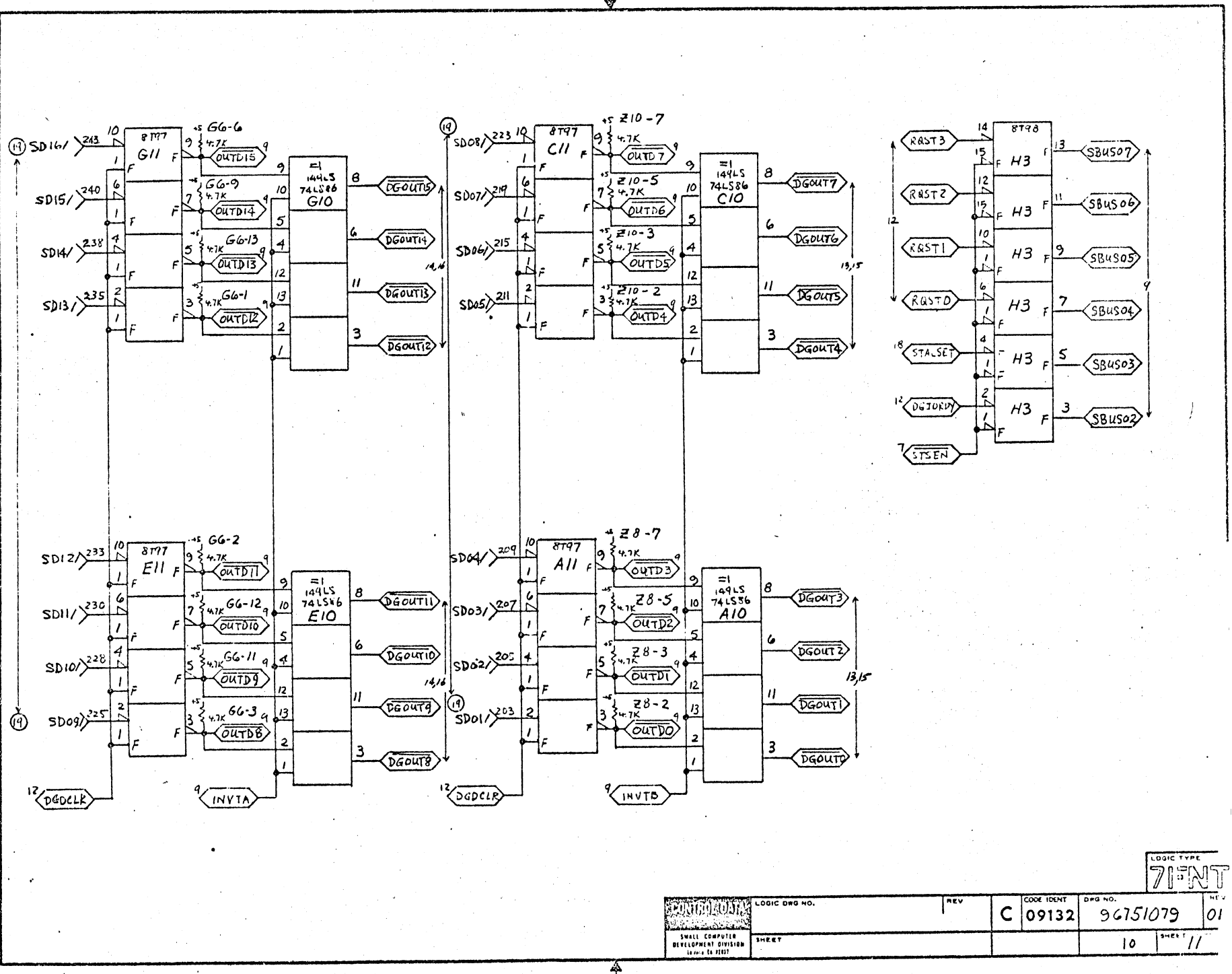

REVISION RECORD
REV
ECO
DESCRIPTION
DFT
DATE
CHK
APPD
K5
M5
L5
L25
E1
L13
K1
K8
K11
K9
K10
K12
L10
L11
M10
L1
KA
ADR01/
ADR02/
ADR03/
ADR04/
AQINT
AQINT-A
INTERRUPT/
BUSIFEN
DGIO
POWFAIL/
MC-S/
BUSRQ·D
71-NT
DIGITAL
SMALL COMPUTER DEVELOPMENT DIVISION
C
09132
96751079
01
7
SHEET 8



CONTROL DATA SMALL COMPUTER DEVELOPMENT DIVISION La Jolla CA 92037	LOGIC DWG NO.	REV	CODE IDENT	DWG NO.
		C	09132	96751079
	SHEET		8	SHEET 9

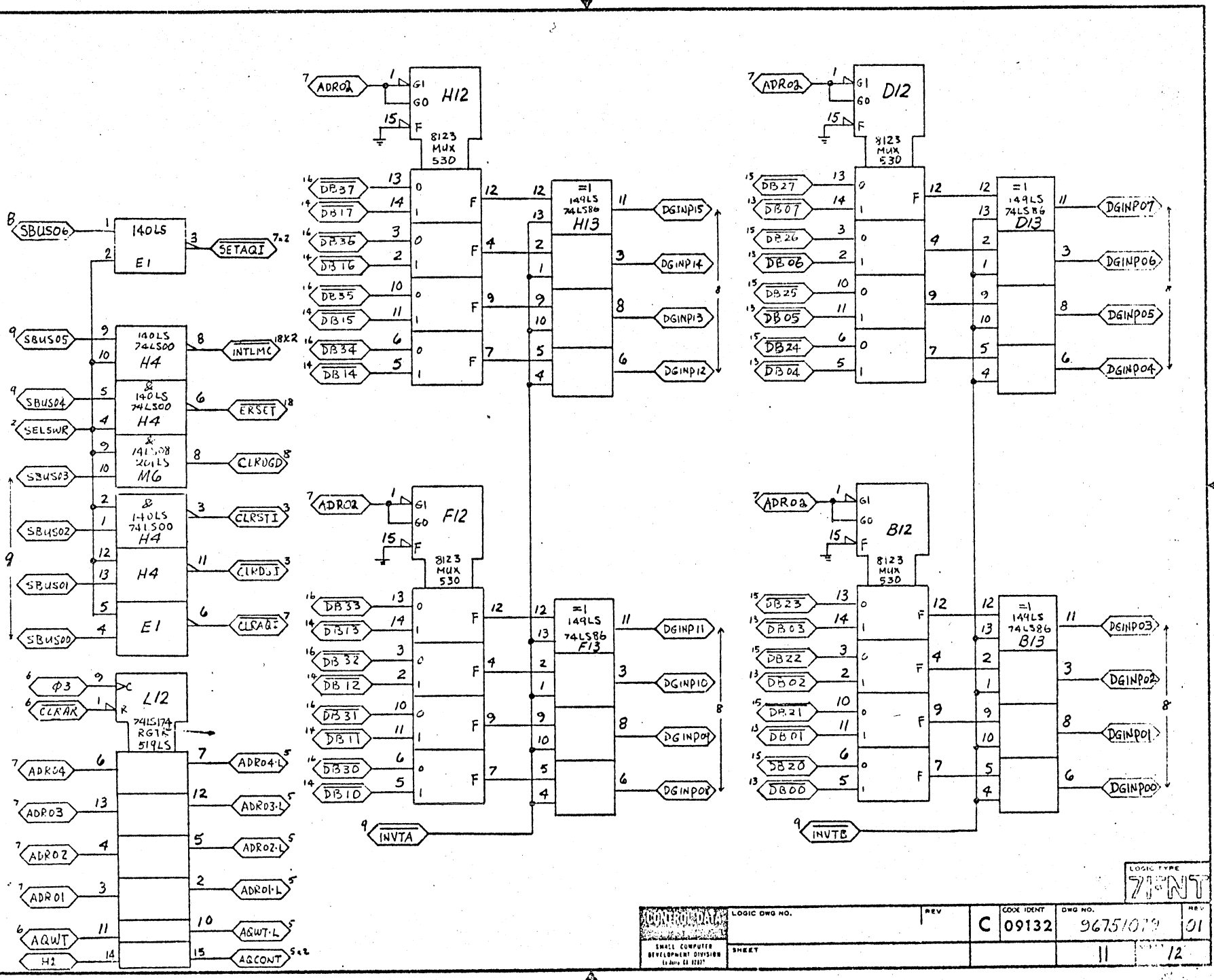
LOGIC TYPE 710


REVISION RECORD
REV | ECO | DESCRIPTION | DATE | CHK | APPD
LO
SEL3
C6
74S258
MUX
H4
SEL3H
H6
74LS175
RGTR
OUTD7
OUTD15
OUTD6
OUTD14
OUTD5
OUTD13
OUTD4
OUTD12
SBUSI7
SBUSI6
SBUSI5
SBUSI4
SBUS07
SBUS06
SBUS05
SBUS04
INPD15
INPD14
INPD13
INPD12
IOREAD
BUSIFEN
D6
8216
RCVR
DRVR
PBUS7
PBUS6
PBUS5
PBUS4
BUSRQ
SEL2L
H5
74LS175
S20LS
RGTR
INTREJ
EXTREJ
INVTA
INVTB
LO
SEL3
A6
74S258
MUX
H1
SEL3H
F6
74LS175
RGTR
OUTD3
OUTD11
OUTD2
OUTD10
OUTD1
OUTD9
OUTD0
OUTD8
SBUSI3
SBUSI2
SBUSI1
SBUSI0
SBUS03
SBUS02
SBUS01
SBUS00
INPD11
INPD10
INPD9
INPD8
IOREAD
BUSIFEN
B6
8216
RCVR
DRVR
PBUS3
PBUS2
PBUS1
PBUS0
BUSRQ
SELIL
K4
74LS175
S20LS
RGTR
BYTE3
BYTE2
BYTE1
BYTE0
71:NT
INTRO DATA
SMALL COMPUTER DEVELOPMENT DIVISION
C
CODE IDENT 09132
DWG NO. 96751079
REV 01
9
SHEET 10



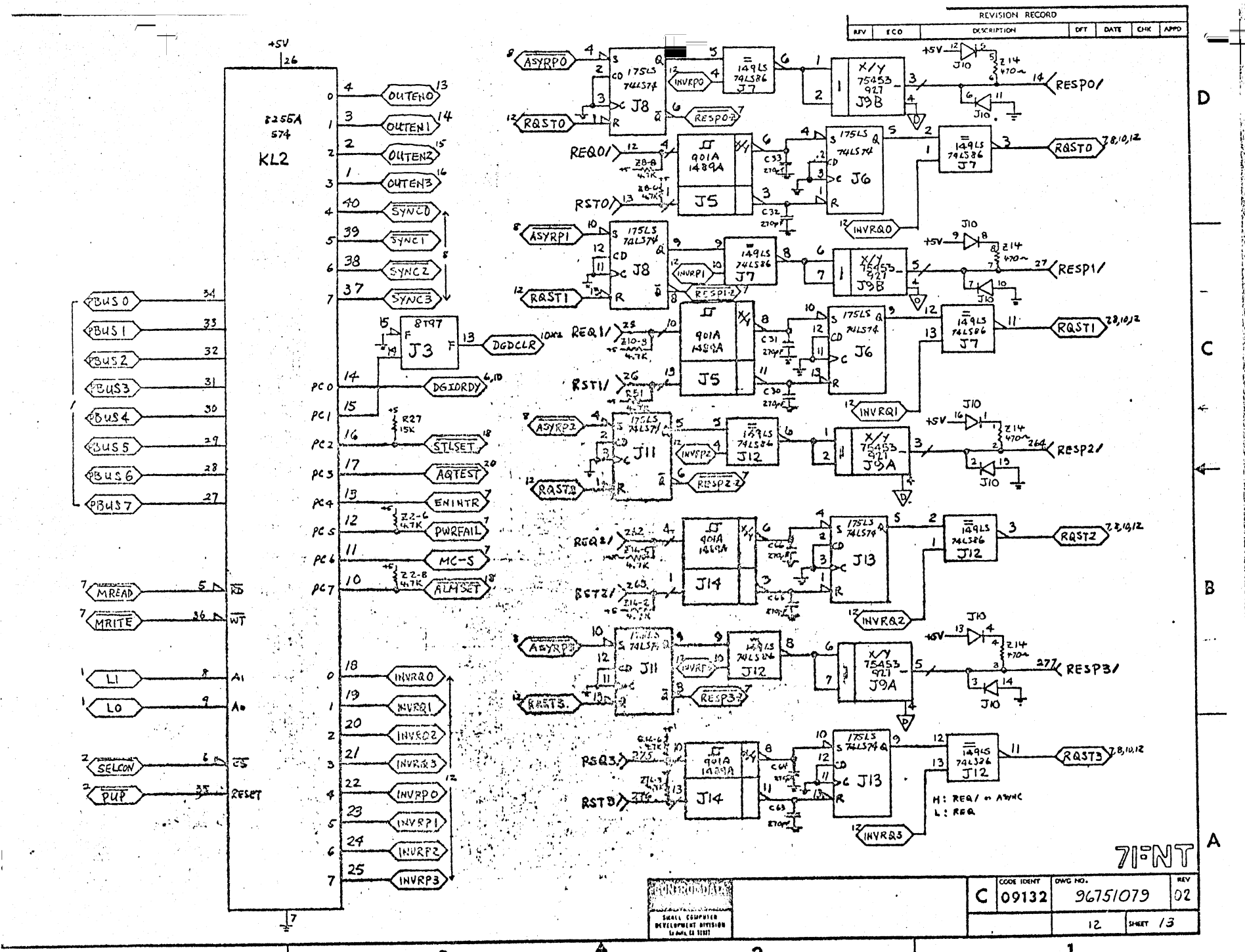
CONTROL DATA SMALL COMPUTER DEVELOPMENT DIVISION	LOGIC DWG NO.	REV	C	CODE IDENT 09132	DWG NO. 96751079 REV 01
	SHEET			10	SHEET 11

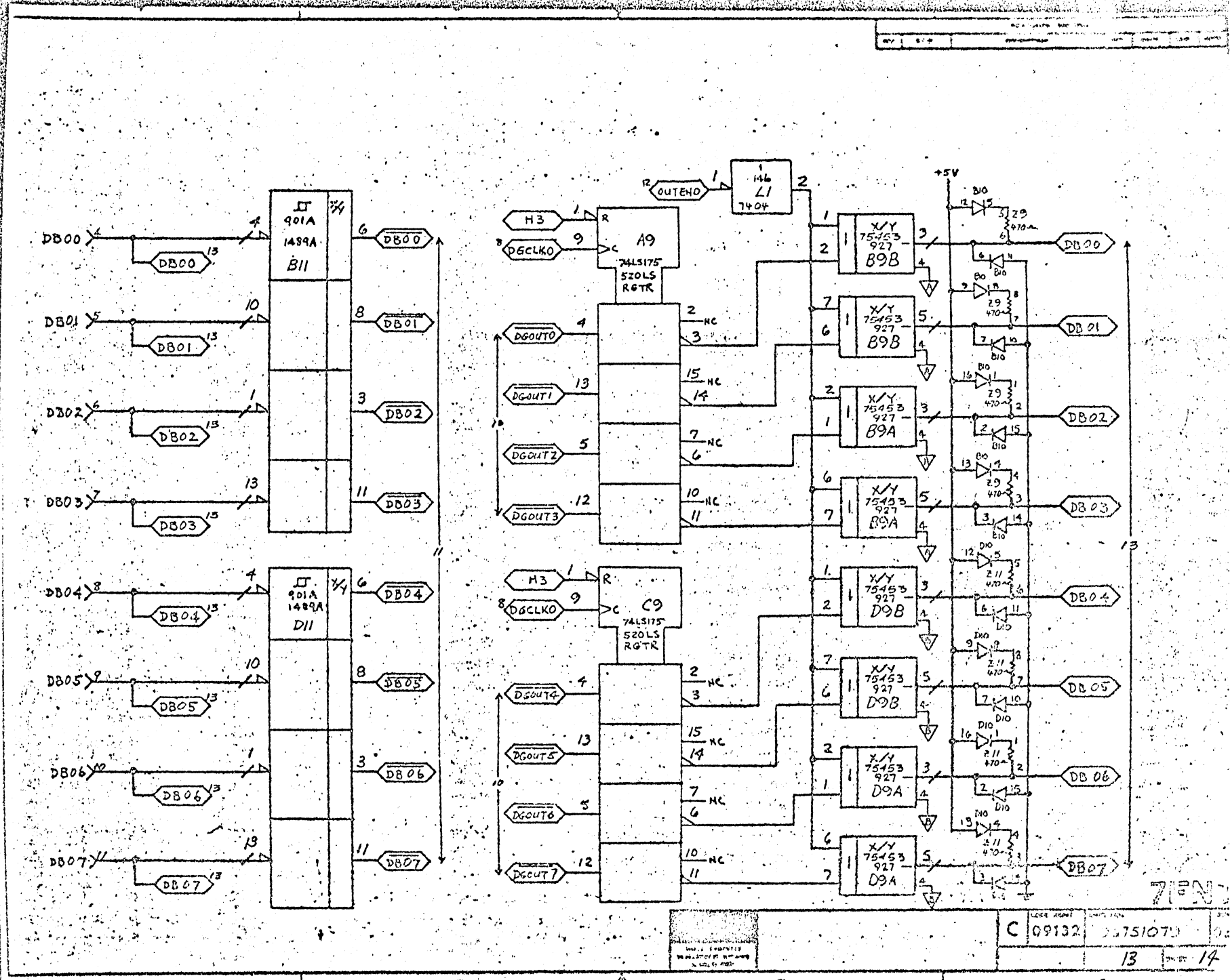
LOGIC TYPE 71NT

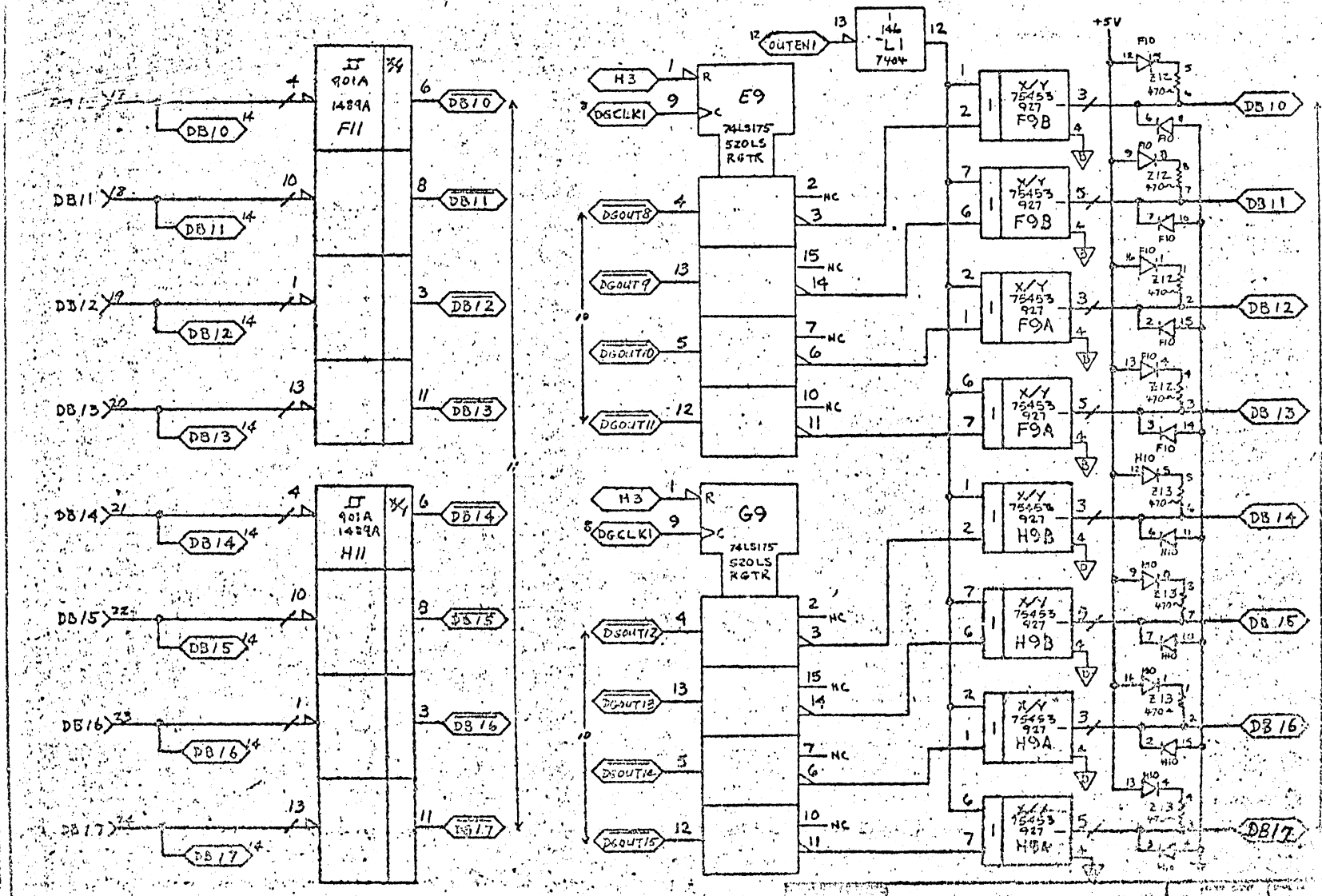


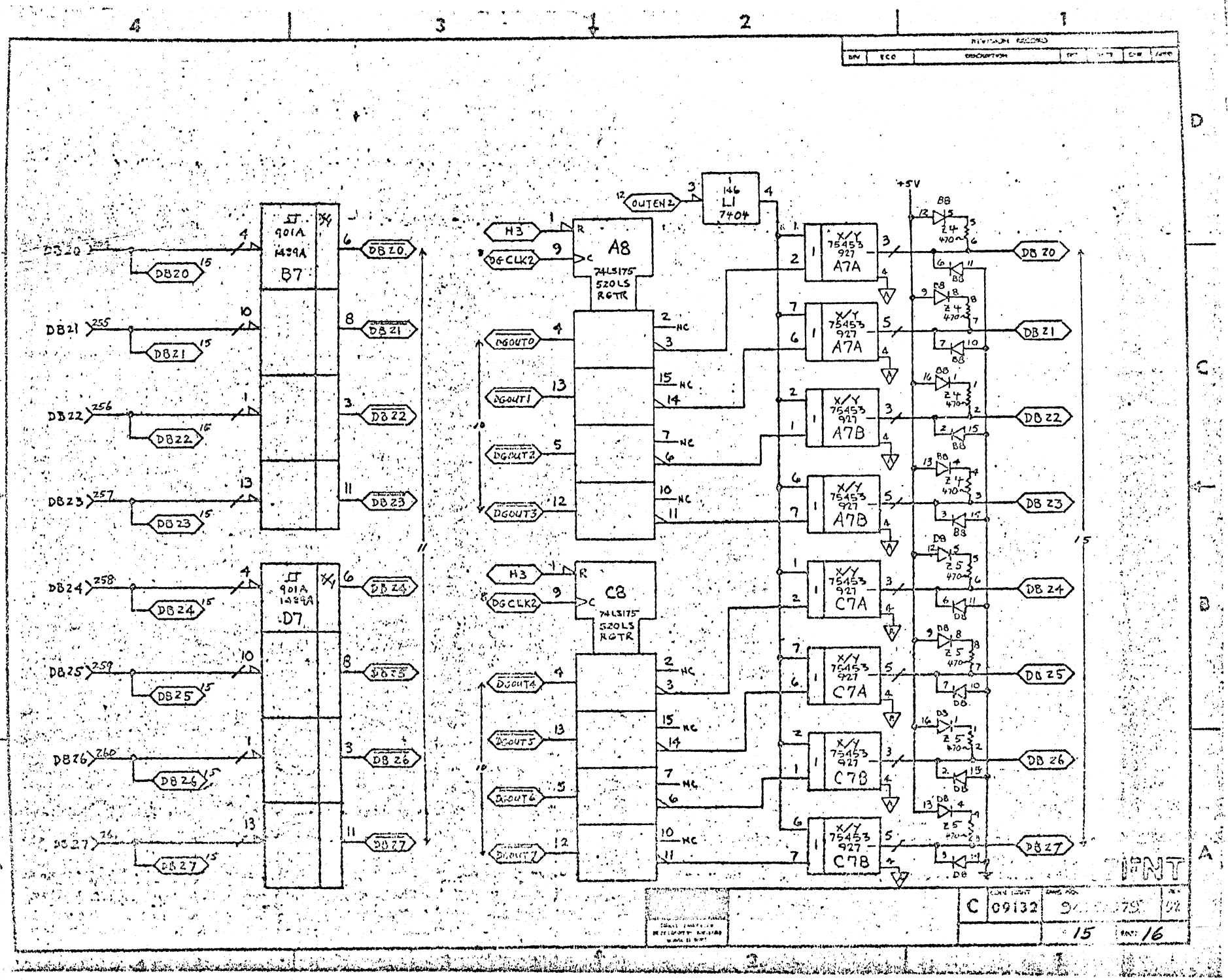
CONTROL DATA SMALL COMPUTER DEVELOPMENT DIVISION	LOGIC DWG NO.	REV	C	CODE IDENT 09132	DWG NO. 9675107? REV 01
	SHEET			11	12

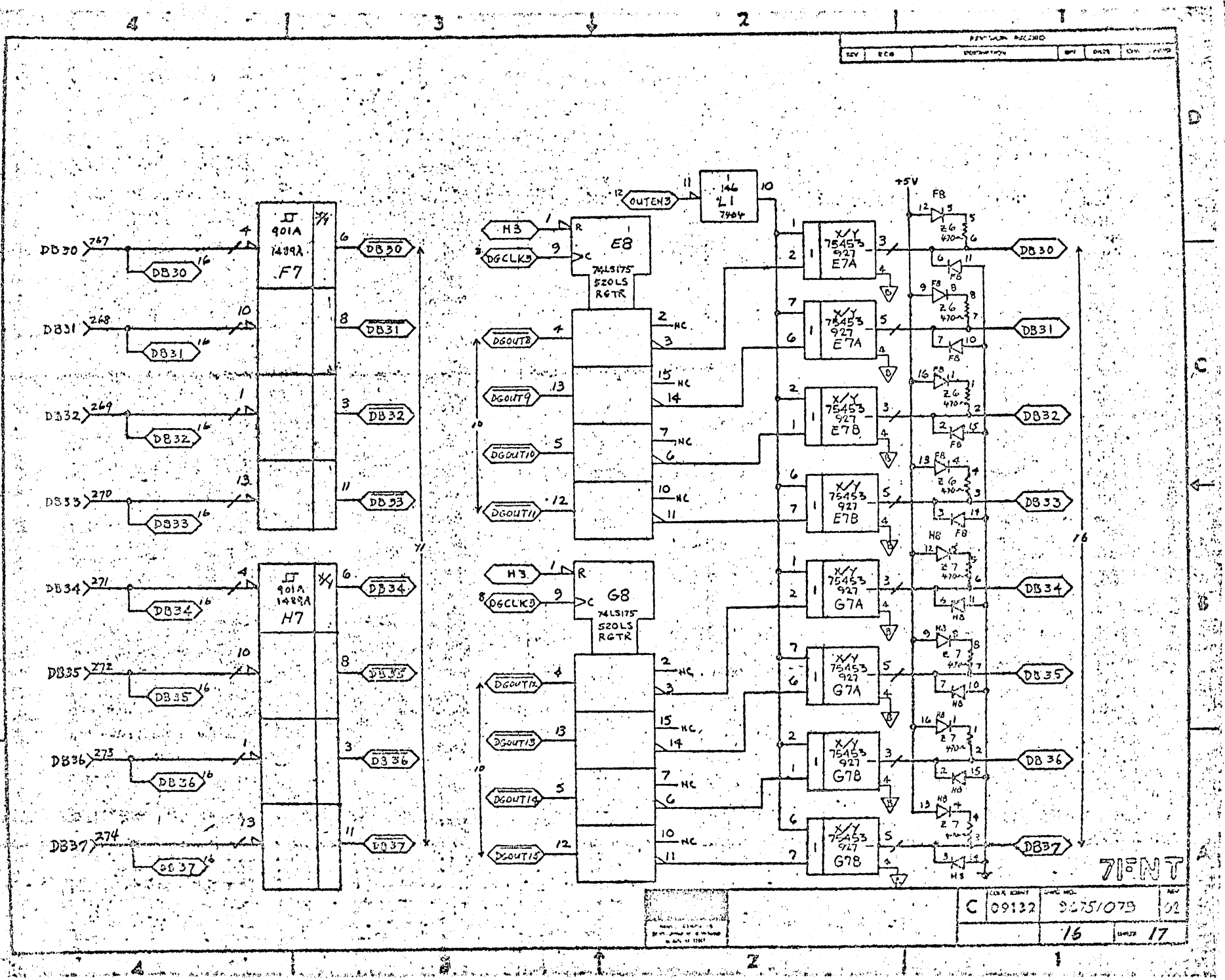
LOGIC TYPE 7:NT

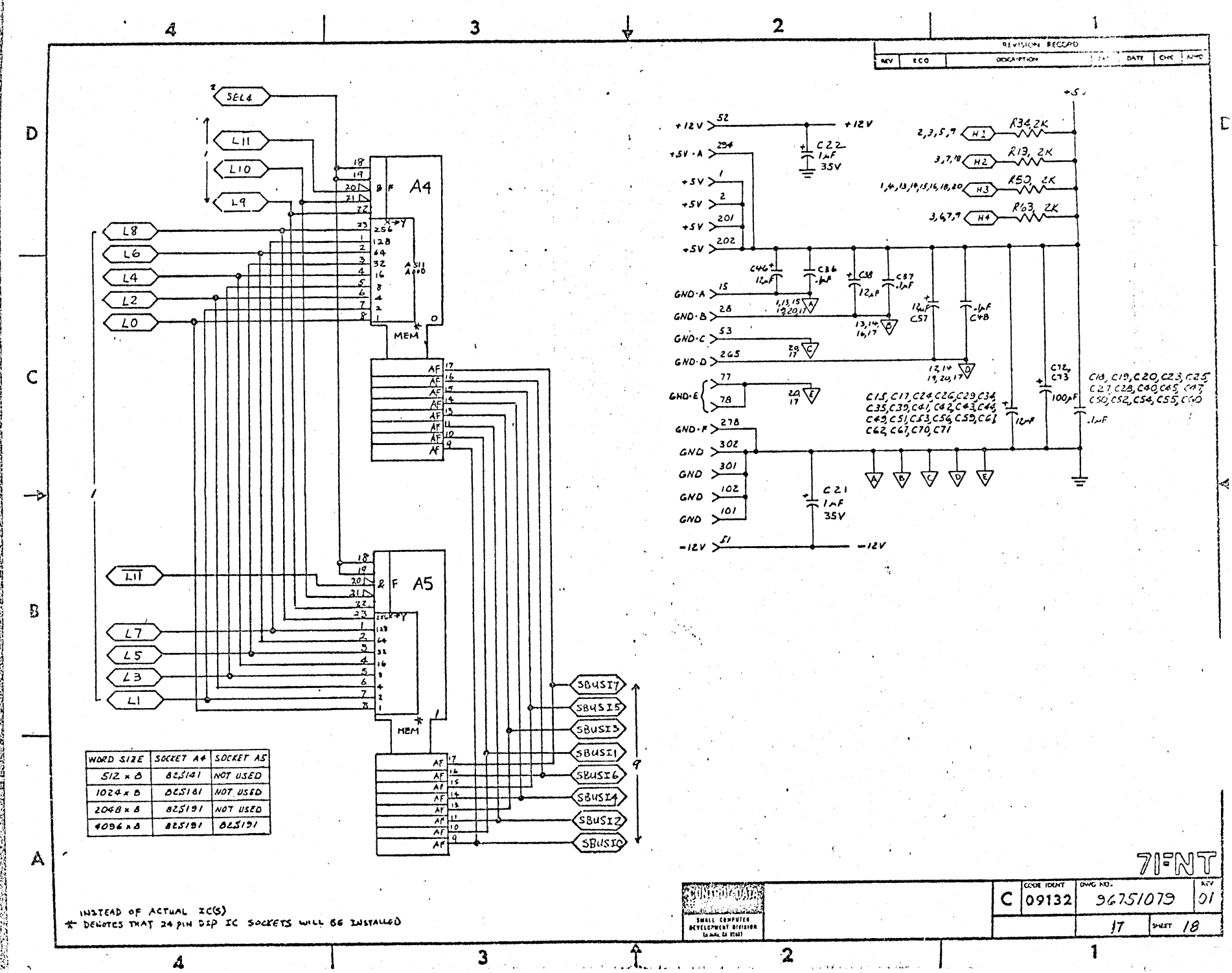

REVISION RECORD
REV ECO DESCRIPTION DFT DATE CHK APPD
+5V
8256A
574
KL2
OUTEN0
OUTEN1
OUTEN2
OUTEN3
SYNC0
SYNC1
SYNC2
SYNC3
PBUS0
PBUS1
PBUS2
PBUS3
PBUS4
PBUS5
PBUS6
PBUS7
8T97
J3
DGDCLR
DGIORDY
STLSET
AQTEST
ENINTR
PWRFAIL
MC-S
ALMSET
MREAD
MWRITE
LI
LO
SELCON
PUP
RESET
INVRQ0
INVRQ1
INVRQ2
INVRQ3
INVRP0
INVRP1
INVRP2
INVRP3
ASYRP0
RQST0
REQ0/
RST0/
ASYRP1
RQST1
REQ1/
RST1/
ASYRP2
RQST2
REQ2/
RST2/
ASYRP3
RQST3
REQ3/
RST3/
RESP0/
RESP1/
RESP2/
RESP3/
RQST0
RQST1
RQST2
RQST3
H: REQ/ = ASYNC
L: REQ
71°NT
CODE IDENT 09132
DWG NO. 96751079
REV 02
SHEET 13


DB00
DB01
DB02
DB03
DB04
DB05
DB06
DB07
901A 1489A B11
901A 1489A D11
H3
DGCLKO
A9
C9
74LS175 520LS RGTR
DGOUT0
DGOUT1
DGOUT2
DGOUT3
DGOUT4
DGOUT5
DGOUT6
DGOUT7
OUTEN0
146 LI 7404
X/Y 75453 927 B9B
X/Y 75453 927 B9A
X/Y 75453 927 D9B
X/Y 75453 927 D9A
+5V
Z9 470Ω
Z11 470Ω
B10
D10


901A 1489A F11
901A 1489A H11
DB10
DB11
DB12
DB13
DB14
DB15
DB16
DB17
E9
G9
74LS175 S20LS RGTR
H3
DGCLKI
DGOUT8
DGOUT9
DGOUT10
DGOUT11
DGOUT12
DGOUT13
DGOUT14
DGOUT15
OUTENI
1/4 LS 7404
+5V
X/Y 75453 927 F9B
X/Y 75453 927 F9A
X/Y 75453 927 H9B
X/Y 75453 927 H9A
Z12 470Ω
Z13 470Ω
F10
H10


DB20
DB21
DB22
DB23
DB24
DB25
DB26
DB27
901A
1489A
B7
D7
H3
DGCLK2
A8
C8
74LS175
S20LS
RGTR
DGOUT0
DGOUT1
DGOUT2
DGOUT3
DGOUT4
DGOUT5
DGOUT6
DGOUT7
OUTEN2
1
146
LI
7404
+5V
X/Y
75453
927
A7A
A7B
C7A
C7B
Z4
470
Z5
470
C
09132


DB30
DB31
DB32
DB33
DB34
DB35
DB36
DB37
901A 1489A F7
901A 1489A H7
H3
DGCLK3
OUTEN3
74LS175 SZOLS RGTR
E8
G8
DGOUT8
DGOUT9
DGOUT10
DGOUT11
DGOUT12
DGOUT13
DGOUT14
DGOUT15
+5V
FB
H8
X/Y 75453 927 E7A
X/Y 75453 927 E7B
X/Y 75453 927 G7A
X/Y 75453 927 G7B
Z.6 470
Z.7 470
TANDY



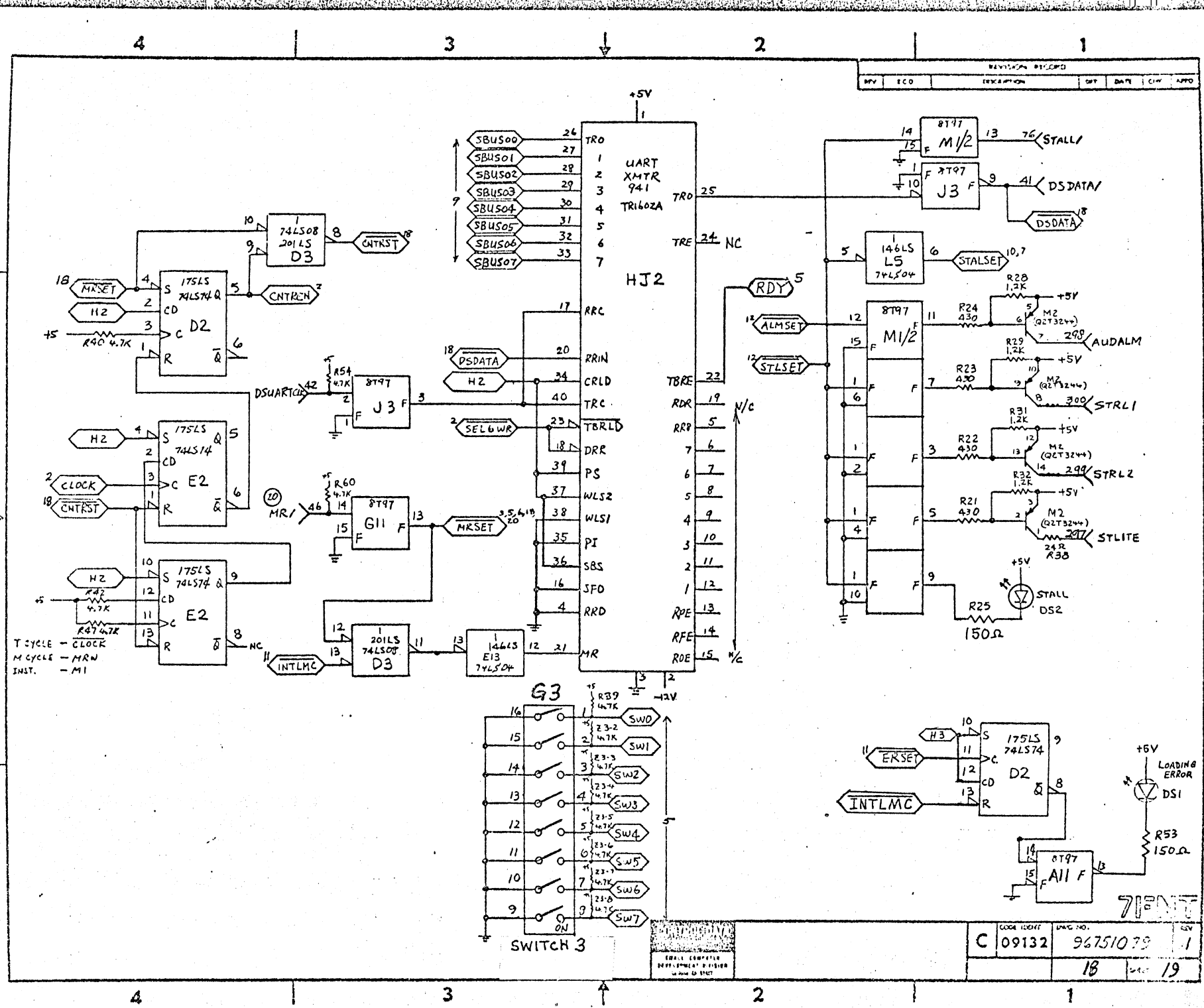
WORD SIZE	SOCKET A4	SOCKET A5
512 x 8	825141	NOT USED
1024 x 8	DCS181	NOT USED
2048 x 8	825191	NOT USED
4096 x 8	825181	DCS191

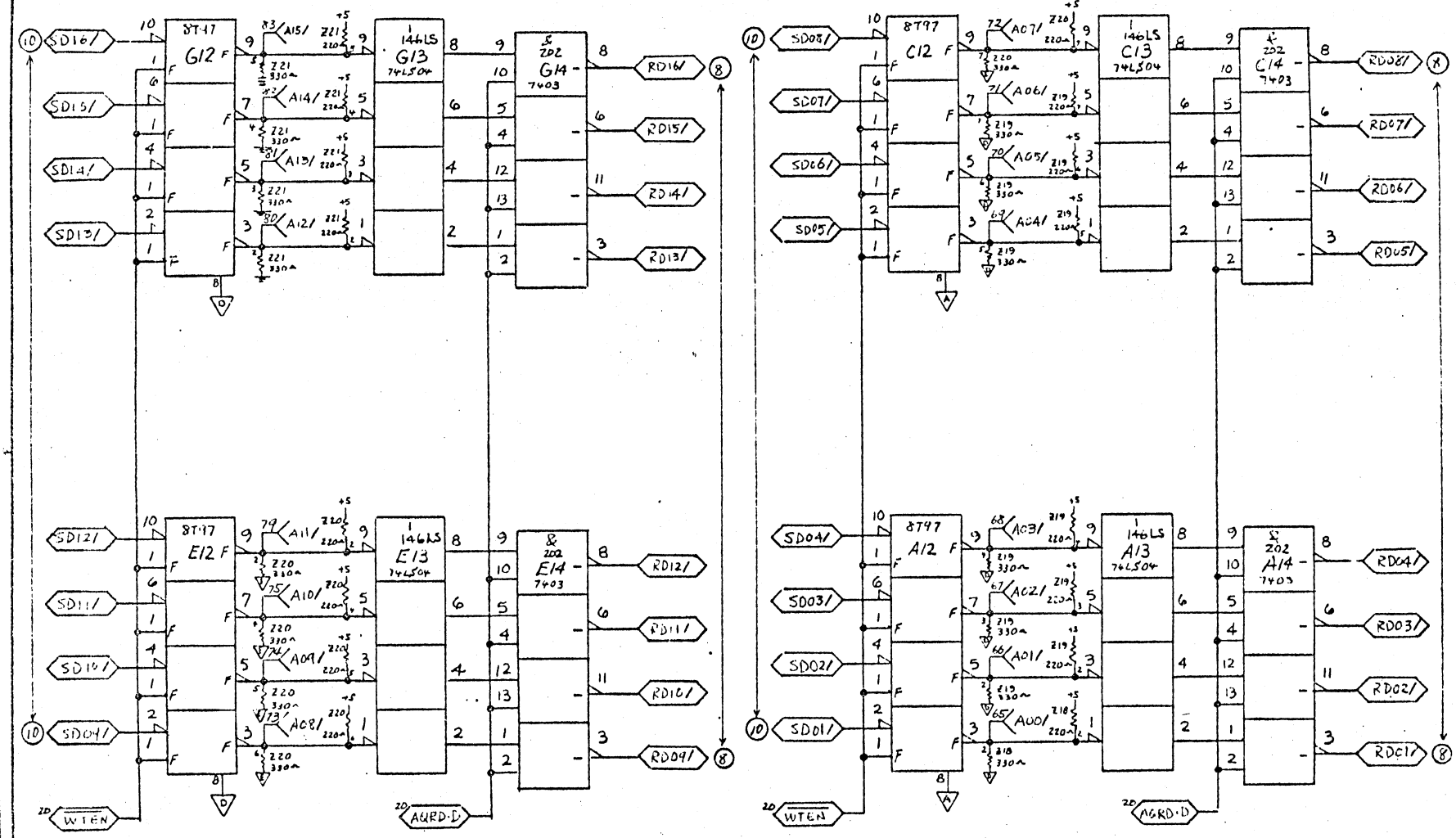
INSTEAD OF ACTUAL IC(S)
* DENOTES THAT 24 PIN DIP IC SOCKETS WILL BE INSTALLED

REVISION RECORD					
REV	ECO	DESCRIPTION	DATE	CHK	APVD

71-NT

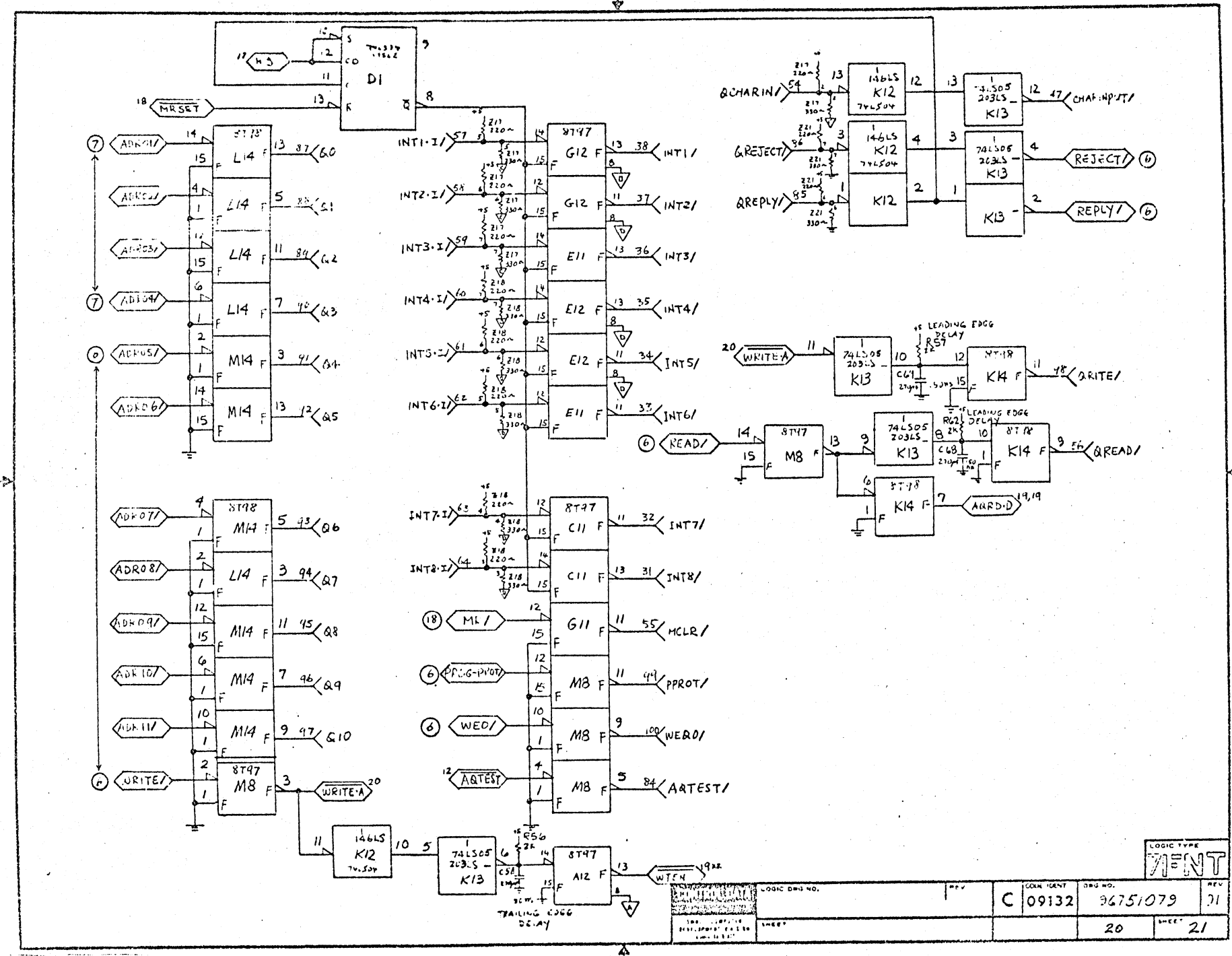
	CODE IDENT	DWG NO.	REV
C	09132	96751079	01
		17 SHEET 18	

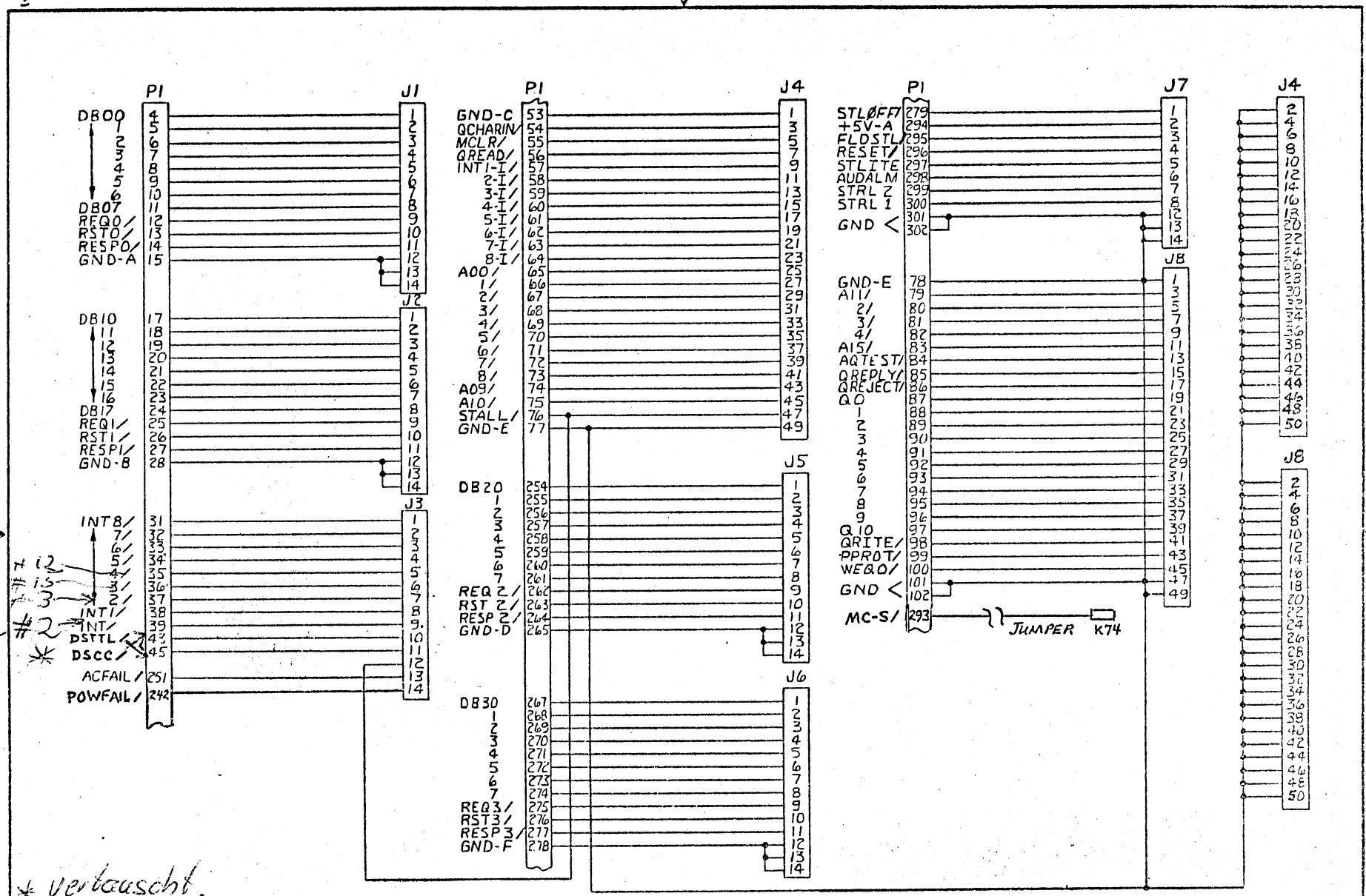

UART XMTR 941 TRI60ZA
HJ2
SBUS00
SBUS01
SBUS02
SBUS03
SBUS04
SBUS05
SBUS06
SBUS07
TRO
TRD
TRE
NC
RRC
RRIN
CRLD
TRC
TBRLD
DRR
PS
WLS2
WLS1
PI
SBS
SFD
RRD
MR
TBRE
RDR
RRP
RPE
RFE
RDE
+5V
-12V
RDY
ALMSET
STLSET
DSDATA
H2
SEL6WR
MRSET
INTLMC
CNTRST
CNTRCN
CLOCK
DSUARTCLK
MR1
STALL/
DSDATA/
STALSET
AUDALM
STRL1
STRL2
STLITE
STALL
LOADING ERROR
ERSET
H3
SWITCH 3
SW0
SW1
SW2
SW3
SW4
SW5
SW6
SW7
ON
T CYCLE - CLOCK
M CYCLE - MRD
INST. - MI
150Ω
249
299
300
298
297
N/C
D1
D2
D3
E2
E13
G11
G3
J3
L5
M1/2
A11 F



LOGIC TYPE 71-NT

LOGIC DWG NO.	REV	CODE IDENT	DWG NO.	RE
	C	09132	9675079	1
SHEET			19	SHEET 20


D1
MRSET
ADR<8>/
ADR<7>/
ADR<6>/
ADR<5>/
ADR<4>/
ADR<3>/
INT1·I/
INT2·I/
INT3·I/
INT4·I/
INT5·I/
INT6·I/
INT7·I/
INT8·I/
INT1/
INT2/
INT3/
INT4/
INT5/
INT6/
INT7/
INT8/
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
WRITE/
WRITE·A
ML/
PROG-PVOT
WE0/
AQTEST
MCLR/
PPROT/
WE0/
AQTEST/
WTEN
R56
2K
TRAILING EDGE DELAY
QCHARIN/
QREJECT/
QREPLY/
CHAR·INP·ST/
REJECT/
REPLY/
WRITE·A
R57
LEADING EDGE DELAY
QRITE/
READ/
R62
QREAD/
AWRD·D
LOGIC TYPE
MENT
LOGIC DWG NO.
REV
C
CODE IDENT
09132
DWG NO.
96751079
REV
01
SHEET
20
SHEET
21



DR 9675262 1	A	B	C	D	E	F
DETACHED LIST	1					
	2					
	3					
	4					
	5					
	6					
	7					

LOGIC TITLE

LOGIC DWG NO | REV.

PWA NO 96752620 | PWB NO 96752619

SMALL COMPUTER DEVELOPMENT DIVISION La Jolla, CA 92037

FIRST USED ON	1855-1	
DR	B. HUFF	3-15-78
CHK	T. Ingram	3-27-78
ENGR	C. Lee	3-29-78
MFG		
APPD		

TITLE: SCHEMATIC DIAGRAM - AUTO RESTART LOADER PADDLE BOARD

CARD POS

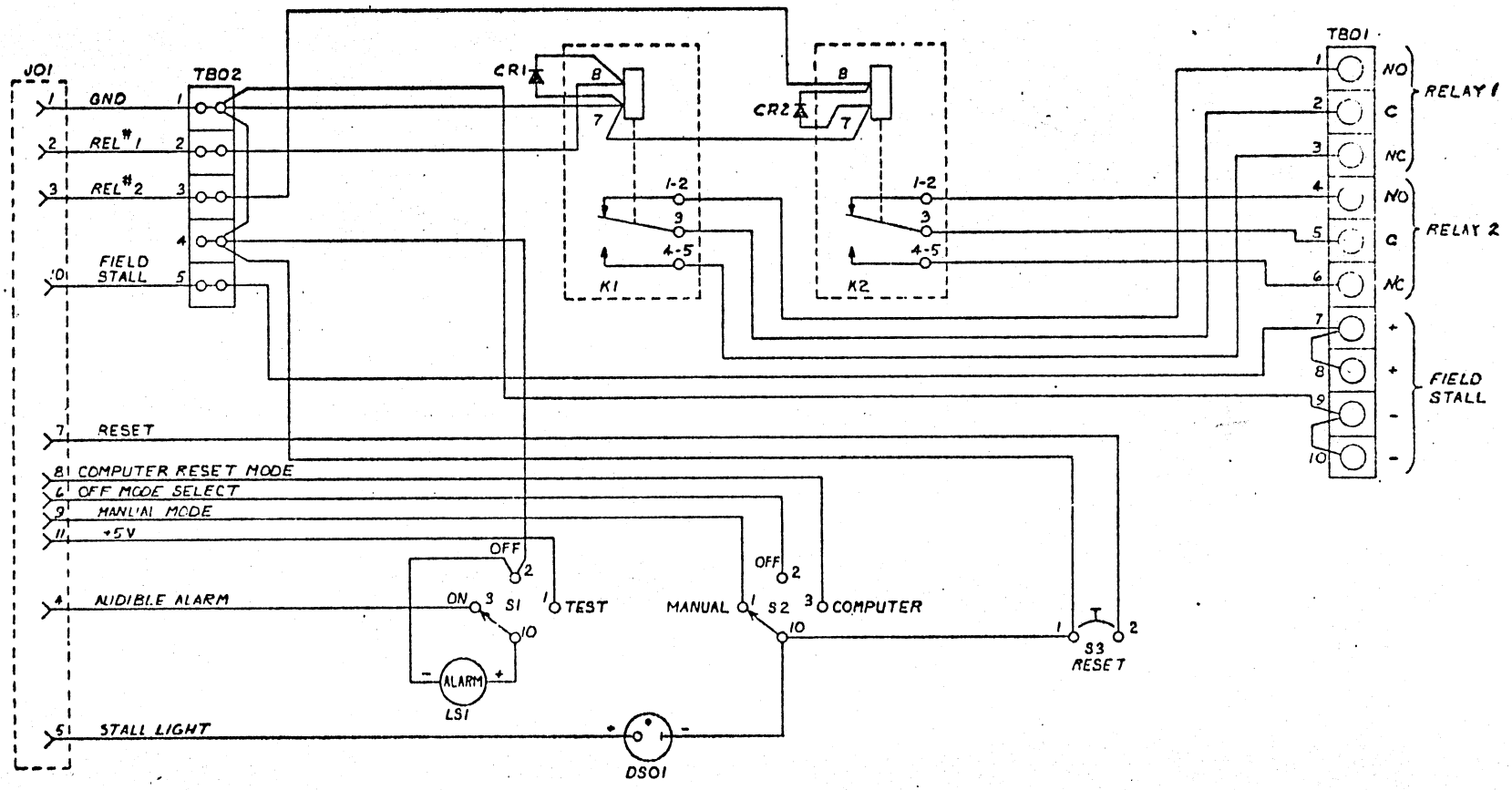
LOGIC TYPE 8HLT

C | CODE IDENT NO 09132 | DRAWING NUMBER 96752621 | REV 01

96752620 | SHEET 1 OF 1

NOTES: UNLESS OTHERWISE SPECIFIED

REVISION RECORD						
REV	ECO	DESCRIPTION	DFT	DATE	CHK	APPD
A		CL.A. RELEASED	[illegible]	2-8-74	[illegible]	[illegible]
B	13568	ADDED CR1 & CR2	[illegible]	[illegible]	[illegible]	[illegible]



REFERENCE DRAWINGS

COMPONENTS, EXCEPT AS NOTED			
	TOLERANCE	VALUE	RATING
RES			
CAP.			

	FIRST USED ON		
DR	L.F. Polatis		2-8-74
CHK	Chuck Brion		2-12-74
ENGR	[illegible]		2-12-74
MFG	[illegible]		
APPD	C. Bynum		2-19-74

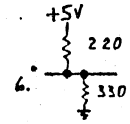
ANALOG - DIGITAL SYSTEMS DIVISION
La Jolla, Calif 92037

TITLE
WIRING DIAGRAM
STALL ALARM PANEL

SIZE	CODE IDENT NO	DRAWING NUMBER
C	09132	88861300

3952130C	SHEET 1	OF 1

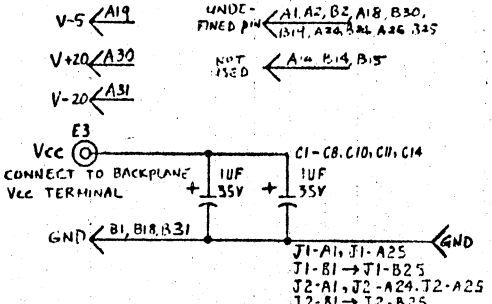
REVISION RECORD						
REV	ECO	DESCRIPTION	DFT	DATE	CHK	APPR
-1		CL C	[illegible]	[illegible]	[illegible]	[illegible]
01	DS18914	CL B. PRE-RELEASED	UM	2-13-78	[illegible]	[illegible]



6. TYPICAL

5. THE P.C. BOARD IS A HALF-SIZED IOM BOARD.
   THE LUG AT THE END OF THE WIRE SHALL BE TIED TO +5V ON THE BACK-PANEL.
4. Vcc (+5V) IS PROVIDED BY A JUMPER WIRE MOUNTED ON THE BOARD.
3. USE RESISTOR NET PAIR 3945 2200 ~~OR 9437 5400~~ FOR RESISTOR PAIRS.
2. ← DENOTES CONNECTOR PINS IN IOM. USE 61PIN CONNECTOR 94243400.
1. ⟩— DENOTES J1 OR J2 CONN. PINS TO THE CPU. USE 2-2x25 RIGHT ANGLE CONN.

NOTES: UNLESS OTHERWISE SPECIFIED



DETACHED LISTS

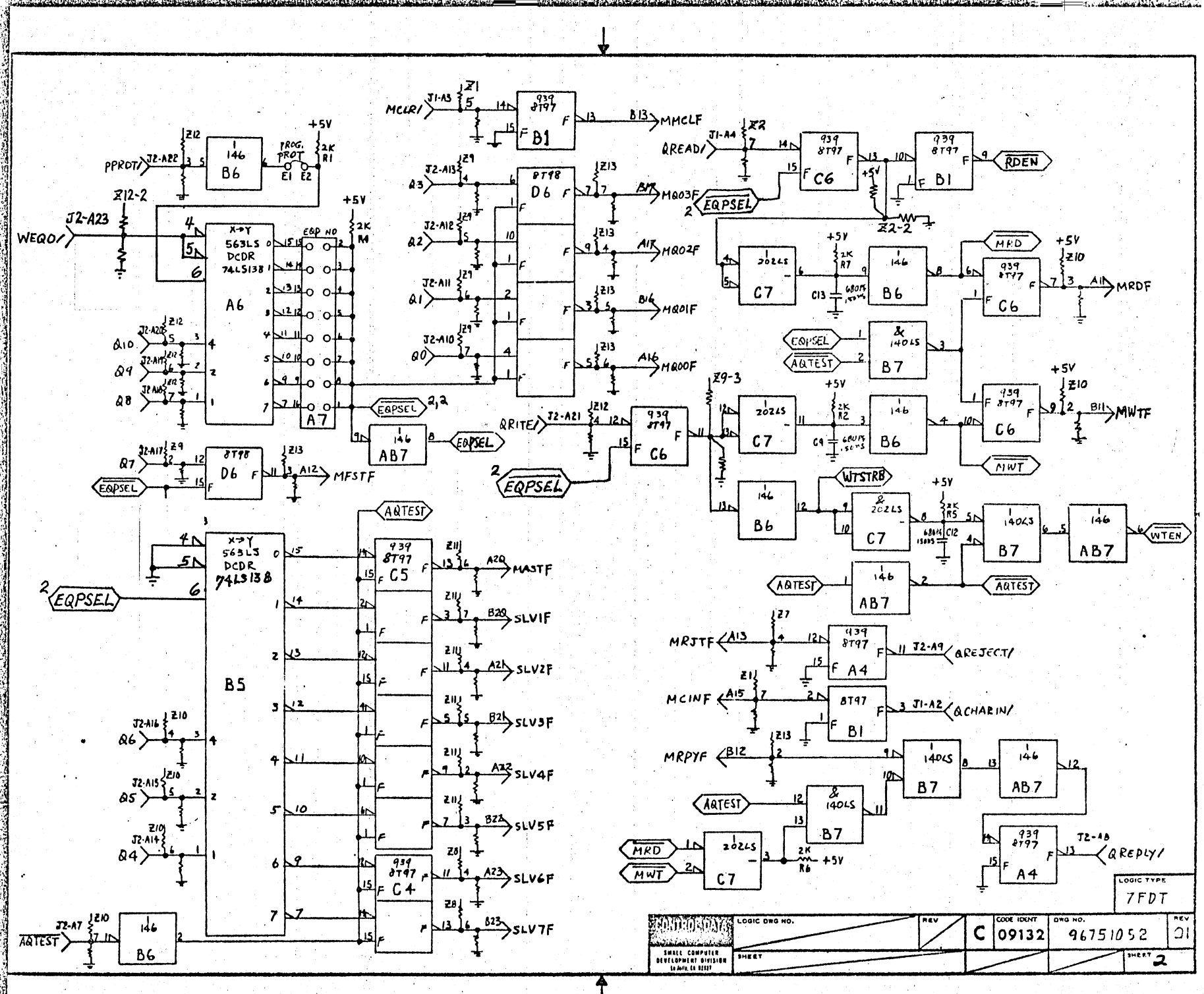
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
3 PLACE ± 2 PLACE ± ANGLES ±
DO NOT SCALE DRAWING
MATERIAL
FINISH

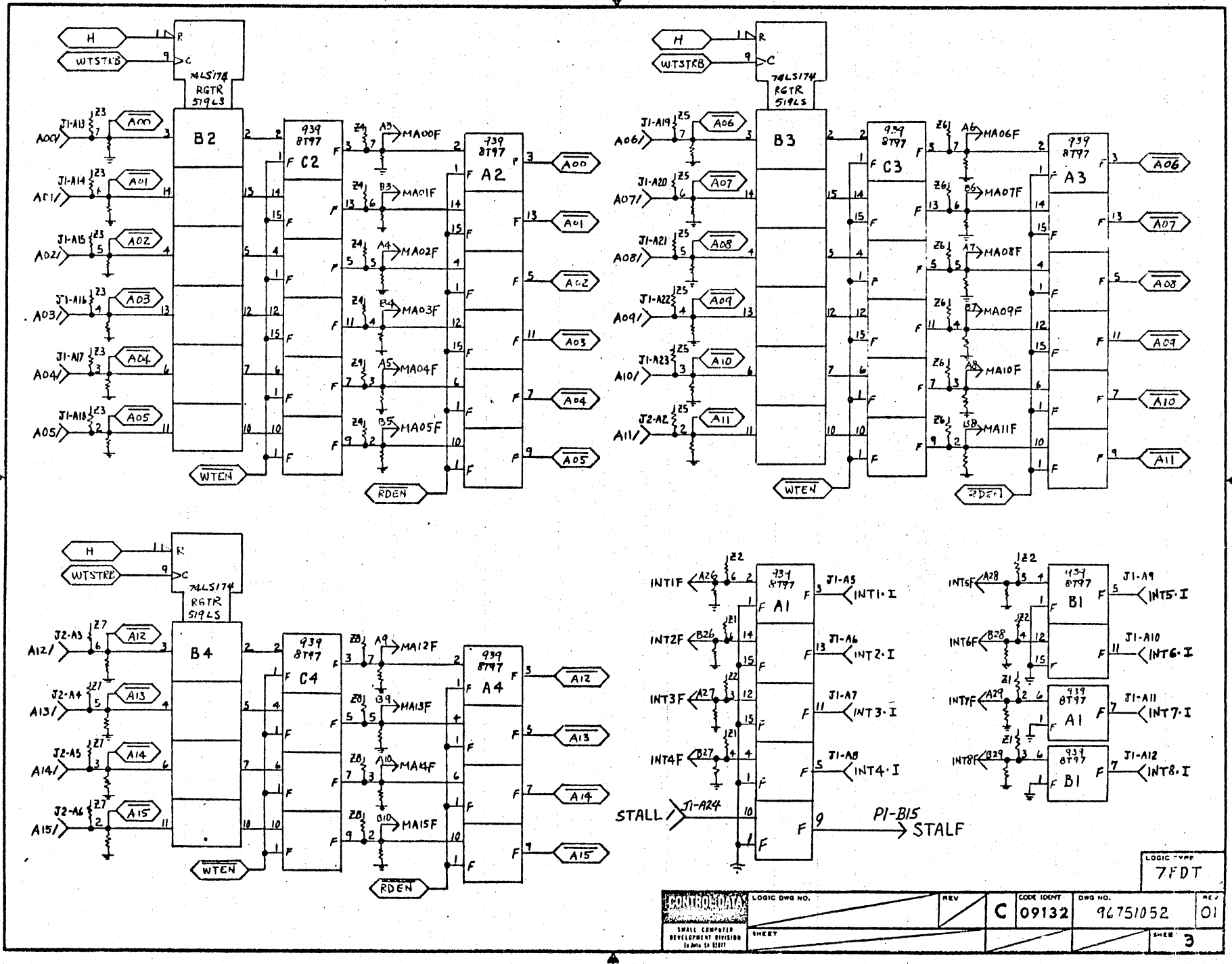
SMALL COMPUTER DEVELOPMENT DIVISION

VENDOR	SHELL/HOLLAND	
DR	[illegible]	8-22-77
CHK	[illegible]	9/20/77
ENGR	[illegible]	9/20/77
MFG		
APPD	[illegible]	9/30/77
ENG	[illegible]	9-26-77

TITLE
LOGIC DIAGRAM
IOM INTERFACE - CYBER 18
7FDT

SIZE	CODE IDENT NO	DRAWING NUMBER
C	09132	96751052
SCALE NONE	96751051	SHEET 1 OF 3


MCLR/
J1-A3
939 8T97 B1
B13
MMCLF
QREAD/
J1-A4
939 8T97 C6
939 8T97 B1
RDEN
EQPSEL
PPROT/
J2-A22
146 B6
PROG. PROT
E1 E2
2K R1
+5V
Z12-2
J2-A23
WEQ0/
X→Y 563LS DCDR 74LS138 A6
EQP NO
A7
2K M
J2-A13
Q3
J2-A12
Q2
J2-A11
Q1
J2-A10
Q0
8T98 D6
B3/
MRQ03F
A1/
MRQ02F
B1/
MRQ01F
A1/
MRQ00F
Q10
Q9
Q8
EQPSEL
146 AB7
Q7
J2-A17
MFSTF
QRITE/
J2-A21
939 8T97 C6
Z9-3
20LS C7
2K R2
C9 680PF .5CMS
146 B6
MRD
939 8T97 C6
A11
MRDF
&
140LS B7
AQTEST
MWT
B11
MWTF
WTSTRB
&
20ZLS C7
2K R5
C12 680PF 1500PF
140L3 B7
146 AB7
WTEN
AQTEST
146 AB7
X→Y 563LS DCDR 74LS138 B5
EQPSEL
AQTEST
939 8T97 C5
939 8T97 C4
A20
MASTF
B20
SLV1F
A21
SLV2F
B21
SLV3F
A22
SLV4F
B22
SLV5F
A23
SLV6F
B23
SLV7F
Q6
Q5
Q4
J2-A16
J2-A15
J2-A14
J2-A7
MRJTF
A13
939 8T97 A4
J2-A9
QREJECT/
MCINF
A15
8T97 B1
J1-A2
QCHARIN/
MRPYF
B12
140LS B7
146 AB7
AQTEST
&
140LS B7
MRD
MWT
20LS C7
2K R6
+5V
939 8T97 A4
T2-A8
QREPLY/
LOGIC TYPE
7FDT
RADIO DATA
SMALL COMPUTER DEVELOPMENT DIVISION
LOGIC DWG NO.
REV
SHEET
C
CODE IDENT
09132
DWG NO.
96751052
REV
01
SHEET
2


H
WTSTRB
74LS174
RGTR
519LS
B2
C2
A2
939
8T97
WTEN
RDEN
B3
C3
A3
B4
C4
A4
B1
A1
STALL
PI-BIS
STALF
LOGIC TYPE
7FDT
CONTROL DATA
SMALL COMPUTER DEVELOPMENT DIVISION
LOGIC DWG NO.
REV
C
CODE IDENT
09132
DWG NO.
96751052
REV
01
SHEET
3

6.1 PREVENTIVE MAINTENANCE

The preventive maintenance (PM) on the ARL, the SAP and the IOM adapter is not required.

6.2 CALIBRATION AND ALIGNMENT

The DC voltage detection levels can be calibrated per 2.1.1.1 Adjustments during the corrective maintenance.

6.3 MAINTENANCE FEATURES

- Read Only Memory (ROM) which contains the ARL controlware is checked with checksum code, whenever power is turned on or the processor is master cleared.
- Programmable ROM furnished by the user is checksum checked before loading operation starts.
- Checksum error from above will be displayed on the error display LED at the ARL top corner.
- Contents of the ARL memory can be read by using station number nine.
- Test mode on the ARL is provided to test the digital I/O bus automatically.
- AQ Test mode signal from the ARL to the IOM adapter provides self testing capability of the IOM bus.

6.3 {Continued}

- "TEST" on the SAP three position switch allows simple SAP test.
- IC sockets are provided to easily replace LSI chips - Z80A microprocessor, 8255 parallel I/O chip, and PROM chips on the ARL.

6.4 MAINTENANCE AID

- Card extender
- Trimmer tweaker
- Volt meter
- Oscilloscope as required

6.5 CORRECTIVE MAINTENANCE

Corrective maintenance will be performed in a repair depot. At the completion of the CM, the equipments shall meet the following requirements:

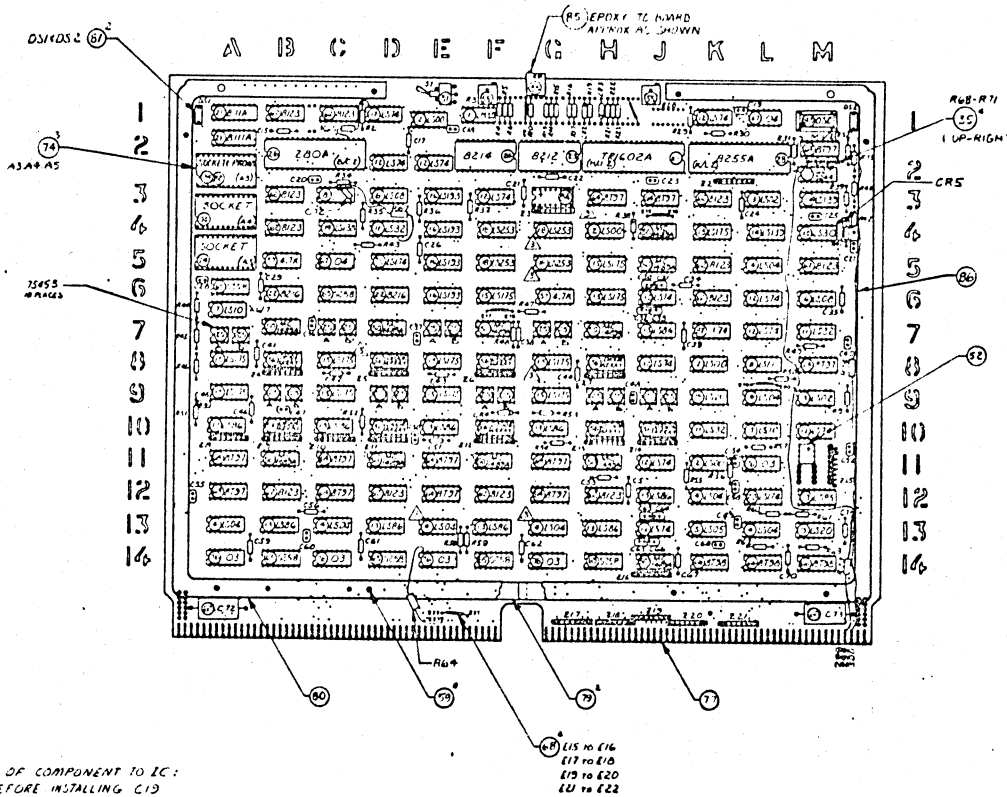
- The ARL shall run all sections of the CRRTMS 2.0 CRTARL test successfully.
- The stall alarm panel shall pass the CRTARL Test 3 Section 3 STALL ALARM UNIT TEST.
- The IOM Adapter shall run the CRTARL Test 4 AQ EXPANSION TEST.

{Refer to Appendix A CRRTMS 2.0 CRTARL description}

7.1 PARTS DATA

This section contains the printed wiring assemblies (PWAs) of the Auto Restart Loader, IOM adapter, and their associated cable assemblies.

Title	
ARL (B1) PWA/P.L.	96870380
ARL (B2) PWA/P.L.	96751078
ARL Paddle Board	96752620
IOM Interface	96751051
Stall Panel Cable Assy.	96754881
IOM Cable Assy.	96752529



FIND NO	REFERENCE DESIGNATIONS
48	C21, C22
43	R16
33	R21
34	R34, R67, R42, R53
37	R32, R33, R33, R40
38	RP3, R31, R36, R45, R56, R57, R62, R63
41	R17
39	P1, P2, P4, R5, P6, P23, R35, P37, P38, R43, R44, R45, R46, R47, R48, R49, R50, R52, R54, R55, R57, R58, R59, R61
42	R14, R15, R24
44	R1
30	R3, R13, R22
46	CR3
49	C42, C44, CR5
54	E17, E18, E19, E20, E21
58	C12, C13, C14
63	C15, C17, C18, C26, C29, C34, C35, C36, C39, C40, C41, C43, C48, C49, C63, C51, C53, C56, C57, C58, C61, C62, C67, C10, C11
69	C30, C31, C32, C33, C58, C60, C61, C64, C65, C66, C68, C69
70	C16, C19, C20, C23, C25, C27, C28, C31, C37, C40, C42, C43, C48, C50, C52, C54, C55, C60
72	E2, E3, E8, E10, E15, E16
75	E4, E5, E6, E7, E9, E11, E12, E13, E14
	R41, R75, R76

1. ASSEMBLE PER CDC SPEC 88518000.
NOTES UNLESS OTHERWISE SPECIFIED

2. WHEN PWA IS SOLD AS A SPARE, FPP 36810780, MUST ACCOMPANY PWA.

3 STRAIGHTEN THE FOLLOWING PINS PARALLEL WITH BOARD: CB-1, G4-13, G5-3, GB-1, G13-10, E13-10, H3-1, H3-15.

4 DUE TO CLOSENESS OF COMPONENT TO IC:
INSTALL IC @ L1 BEFORE INSTALLING C19
INSTALL IC @ L3 BEFORE INSTALLING C2*
INSTALL IC @ F7 BEFORE INSTALLING R40 OR C38.

		PW ASST - AUTO RESTART LOADER (SMT)	
	D	09132	36870580

3

DWN	[illegible]	7-5-78	DATA SYSTEMS LA JOLLA DIVISION
CHKD	G. LAGE	7-31-78	
ENG	C. Lee	7/4-78	CODE IDENT 09132
MFG			
APPR	O. [illegible]	7-31-78	

TITLE PWA-AUTO RESTART LOADER (8JHT)

FIRST USED ON FV679B (QSE 20030)

PREFIX	DOCUMENT NO.	REV.
PL	96870380	01

SHEET 1 OF 4

SHEET REVISION STATUS

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	CHK'D	APP
01	DS18964	[illegible]	B.H.	8-31-78	G.L	AW

NOTES:

DETACHED LISTS

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

S = SPARE PAR
N = NON SPARE PARTS

SH 2

HF

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER
96870380	01	CLR	D	PWA-AUTO RESTART LOADER 8JHT	DS	FV6793	08/27/78	08/27/78	~~1~~ / ~~3~~

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PN NC	S OR N
86	A	15006509	4000	IN	WIRE-ELEC W/W TEFZEL 30GA WHT	IN			PPP1		N
1	A	15126600	100	PC	I.C. M-QUAD COMPAR. DIP LM339	IN					N
25	A	15128200	1800	PC	I.C. 75453	IN					N
2	A	15144900	400	PC	IC TTL QUAD 2-IN NAND 74LS00	IN			PPP4		N
3	A	15145000	200	PC	IC TTL QUAD 2-INPUT NOR 74LS02	IN			PPP4		N
4	A	15145100	800	PC	IC TTL HEX INVERTER 74LS04	IN			PPP4		N
5	A	15145300	100	PC	IC TTL HEX INVERTER 74LS05	IN			PPP4		N
6	A	15145400	200	PC	IC TTL QUAD 2INPUT AND 74LS08	IN			PPP4		N
7	A	15145600	200	PC	IC TTL TRPL 3INPUT NAND 74LS10	IN			PPP4		N
8	A	15145700	200	PC	I.C. 74LS11	IN					N
9	A	15145900	200	PC	IC TTL DUAL 4INPUT NAND 74LS20	IN			PPP4		N
10	A	15146100	100	PC	I.C. 74L530	IN					N
11	A	15146200	300	PC	IC TTL QUAD 2INPUT OR 74LS32	IN			PPP4		N
12	A	15146300	1200	PC	IC TTL DUAL D-TYPE F/F 74LS74	IN			PPP4		N
13	A	15146400	1000	PC	IC TTL QUAD 2INPUT EXC 74LS86	IN			PPP4		N
14	A	15146600	200	PC	IC-74LS139 DECODER TTL DUAL	IN			PPP4		N
15	A	15146900	1200	PC	IC-TTL,LATCH 4 BIT 74LS175	IN			PPP4		N
16	A	15147000	400	PC	IC COUNTER TTL 4-BIT 74LS193	IN			PPP4		N
17	A	15147200	100	PC	IC-74LS85 TTL 4 BIT COMPARATOR	IN			PPP4		N
18	A	15147300	400	PC	IC-MUX DUAL 4-IN TRI 74LS253	IN			PPP4		N
19	A	15147400	100	PC	IC, DECODER-STTL 74LS138	IN			PPP4		N
20	A	15147500	200	PC	IC LATCH-STTL 6-BIT D-TYPE	IN			PPP4		N
21	A	15151600	200	PC	I.C. 8111A	IN			PPP4		N
22	A	15155300	200	PC	IC-8216 4 BIT BI-DIR BUS DRVR	IN			PPP4		N
23	A	15155400	100	PC	IC-8212 8 BIT I/O PORT	IN			PPP4		N
24	A	15156300	100	PC	IC-8214 PRIORITY INTERRUPT CNT	IN			PPP4		N
26	A	15163201	100	PC	IC Z80A MOS 8 BIT CPU	IN			PPP4		N
27	A	15163224	100	PC	TRANSISTOR ARRAY-PNP HIGH CUR	IN			PPP4		N
28	A	15164427	100	PC	IC-8255A	IN			PPP4		N
30	C	17705912	300	PC	RES FXD .25W 0.1 MEG OHMS	IN			PPP4		N
31	C	18696001	100	PC	SWITCH TOGGLE	IN			PPP4		N
32	C	24500024	300	PC	RES FXD .25W 24 OHMS	IN			PPP4		N
33	C	24500036	100	PC	RES FXD .25W 75 OHMS	IN			PPP4		N
35	C	24500054	400	PC	RES FXD .25W 430 OHMS	IN			PPP4		N
36	C	24500055	400	PC	RES FXD .25W 470 OHMS	IN			PPP4		N
37	C	24500065	400	PC	RES FXD .25W 1200 OHMS	IN			PPP4		N

PROJECT ENGINEER

C LEE

SCMD

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PAR
N = NON SPARE PARTS

SH 3

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER
96870380	01	CLB	D	PWA-AUTO RESTART LOADER 8JHT	DS	FV679B	08/27/78	08/27/78	~~2/3~~

MF

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	DN NC	S OR N
38	C	24500070	800	PC	RES FXD .25W 2000 OHMS	IN			PPP4		N
39	C	24500079	2400	PC	RES FXD .25W 4700 OHMS	IN			PPP4		N
41	C	24500083	100	PC	RES FXD .25W 6800 OHMS	IN			PPP4		N
42	C	24500087	300	PC	RES FXD .25W 10000 OHMS	IN			PPP4		N
43	C	24500089	100	PC	RES FXD .25W 12000 OHMS	IN			PPP4		N
44	C	24500091	100	PC	RES FXD .25W 15000	IN			PPP4		N
46	C	24503804	100	PC	DIODE SILICON, ZENER	IN			PPP4		N
48	C	24505229	200	PC	CAP,FXD SOL TA 35V 1.0UF 10PCT	IN			PPP4		N
49	A	25175800	300	PC	DIODE(1N914)	IN			PPP4		N
50	A	36186501	1100	PC	IC CHIP TYPE 1489	IN			PPP4		N
84	A	39396501	100	PC	SWITCH,LOW PROFILE DIP-SPST	IN			PPP4		N
52	A	39396502	100	PC	SWITCH, LOW PROFILE DIP-SPST 4	IN			PPP4		N
54	A	39452200	500	PC	RES NETWORK-VOLTAGE DIVIDR-SIP	IN			PPP4		N
55	A	39772108	300	PC	POT-CERMET .5W 3/8 SQ 5K OHM	IN			PPP4		N
56	A	50241800	900	PC	DIODE ARRAY, 8, DIC16	IN					N
85	A	62019900	01	OZ	EPOXY, 2 PART 5 MIN(CLEAR)TUBE	IN			PPP3		N
57	A	75009934	200	PC	RES PKG-THK FILM,4.7K OHMS	IN			PPP4		N
58	A	84996725	300	PC	CAP,CER 100V 680 PF	IN			PPP4		N
59	A	88812400	800	PC	RIVET-SEMI-TUBULAR,BRS .312 LG	IN			PPP4		N
60	A	88880500	200	PC	CAP-FIXED AL,16VDC,100UF	IN			PPP4		N
61	A	88881000	100	PC	IC-TR1602A (UART) MOS DATA I/F	IN			PPP4		N
87	A	88882800	100	PC	IC 74174 TTL HEX D F/F W/CLEAR	IN			PPP4		N
62	A	88896000	1200	PC	IC 8123 TTL TRI-STATE 2-IN MUX	IN			PPP4		N
63	A	88897800	2500	PC	CAP-FIXED SOLID TANT,6VDC,12UF	IN			PPP4		N
64	A	88916800	1200	PC	IC 8T97 TTL TRI-STATE HEX BFR	IN			PPP4		N
65	A	88920800	600	PC	IC 74S258 TTL QUAD 1-L SEL/MUX	IN			PPP4		N
66	A	88920900	300	PC	IC 8T98 TTL TRI-ST HEX BFR/INV	IN			PPP4		N
67	A	88924500	200	PC	IC 7404 TTL HEX INVERTER	IN			PPP4		N
68	A	88945400	400	PC	JUMPER 24AWG TEF INSULATED .50	IN			PPM4		N
69	A	89636100	1100	PC	CAP,FXD CER 270PF	IN			PPP4		N
70	A	89636157	1800	PC	CAP,FXD CER .1 MFD 50 VDCW	IN			PPP4		N
72	A	91938552	600	PC	RESISTOR MODULE 8 PIN	IN			PPP4		N
74	C	94260302	300	PC	SOCKET I.C.	IN					N
75	A	94375103	900	PC	RES NETWORK, 8PIN SIP 470 OHMS	IN			PPP4		N
76	A	96744154	500	PC	IC 7403 TTL QUAD 2-IN POS NAND	IN			PPP4		N
79	C	96752479	200	PC	INSULATOR-CARD FRAME	IN			PYP4		N

PROJECT ENGINEER
C LEE

SCMD

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE COD
S = SPARE PAI
N = NON SPARE PARTS

SH 4

MF

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER
96870380	01	CLB	D	PWA-AUTO RESTAPT LOADER 8JHT	DS	FV679B	08/27/78	08/27/78	~~3/ 3~~

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PN NC	S OR N
80	C	96752480	100	PC	FRAME-CARD (MODIFIED)	IN			PYP4		N
81	A	96752541	200	PC	INDICATOR-LED	IN			PPP4		N
82	A	96754700	100	PC	IC-8K ROM,AUTO RESTART,LOC. A3	IN			KTM4		N
83	A	96860401	100	PC	OSCILLATOR-HBD CLK,16.0000 MHZ	IN			PPP4		N
77	D	96870180	100	PC	PWB-AUTO RESTART LOADER	IN					N
78	C	96870580	REF	PC	LOGIC DIAG-AUTO REST LOAD 8JHT	IN					N

NUMBER OF LINE ITEMS = 78
HIGHEST FIND NUMBER = 87

PROJECT ENGINEER

C LEE

SCND

AA 27[illegible] REV 7 75

DSN	[illegible]	7-3-	
CHK	S. LARA-F	7-31-	
ENG	C. LOE	7-30-	DATA SYSTEMS LA JOLLA DIVISION
MFG			
APPR	J. HILL	7-31-78	CODE IDENT 09132

TITLE PWA - AUTO RESTART LOADER (8JHT)

PREFIX	DOCUMENT NO.	REV.
DN	96870380	01

FIRST USED ON FV679B (QSE 20030)

SHEET 1 OF 4

SHEET REVISION STATUS

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	CHK	APP
01	DS18964	CTL B. PRE-RELEASED	BH	7-31-78	G.L.	AW

NOTES:

DETACHED LISTS

	DATA SYSTEMS LA JOLLA DIVISION LA JOLLA, CA. 92037	CODE IDENT 09132	SHEET 2	DN	DOCUMENT NO. 96870380	REV 01

A. CUT CLAD AS FOLLOWS:
(COMPONENT SIDE)

1. C5-5
2. D1-1
3. D1-3
4. F1-1
5. F1-5
6. F1-10
7. E5-2
8. E9-1
9. G2-14 (2 PLACES)
10. J1-1 (2 PLACES)
11. J3-2
12. J3-10
13. J3-11
14. K1-8
15. K8-3
16. L12-3
17. L1-4
18. L13-2
19. M2-8
20. M2-14
21. M13-9
22. M8-7
23. M10-9
24. M10-11
25. M11-E
26. H3-12
27. F2-15

27. A9-1 TO R51
28. R14 TO R15
29. R15 TO CR1

B. CUT CLAD AS FOLLOWS:
(NON-COMPONENT SIDE)

1. C1-2
2. D3-2
3. E9-1
4. F1-4
5. F1-7
6. F1-8
7. F1-9
8. F1-10
9. F1-12
10. F1-13
11. F1-14
12. H3-11
13. H3-13
14. H3-14
15. J1-7
16. J3-1
17. J3-9
18. J3-3 (2 PLACES)
19. K1-9
20. K1-10
21. K8-1
22. K11-10
23. L1-2
24. L1-10
25. L1-12
26.
27. M10-11
28. M10-12
29. M10-13 (2 PLACES)
30. M12-4
31. M12-6
32. M12-10
33. M12-11
34. M12-12
35. M12-13
36. M12-14
37. M13-8
38. A9-1

DATA SYSTEMS LA JOLLA DIVISION LA JOLLA, CA. 92037	CODE IDENT 09132	SHEET 3	DN	DOCUMENT NO: 96870380	REV 01

C. ADD WIRE AS FOLLOWS (F/N86) COMPONENT SIDE:

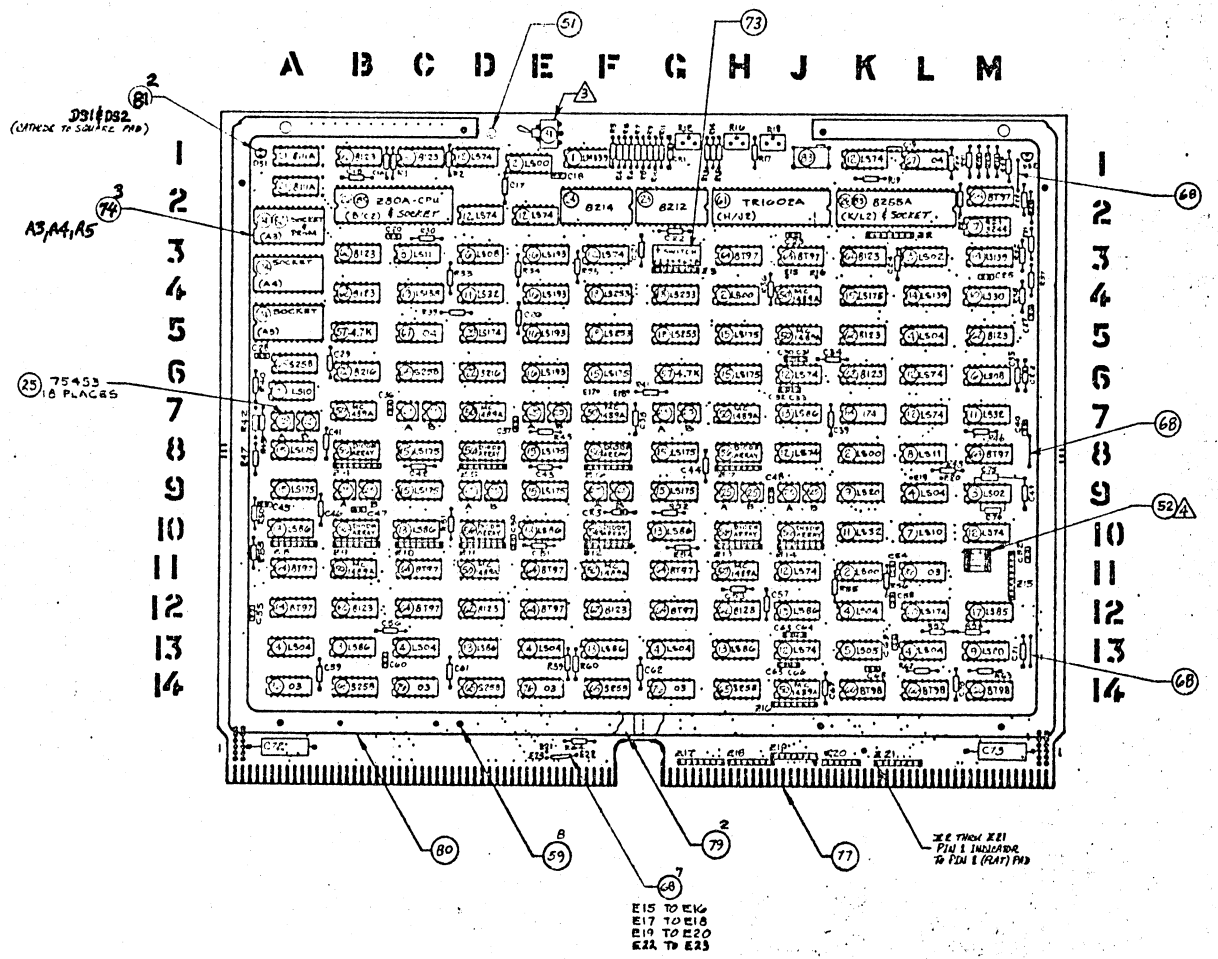
1.	A8-1	TO	C8-1	28.	G13-10	TO	G13-11	55.	L1-6	TO	F2-19
2.	A7A-1		R51 (POINT A)	29.	G2-14		F2-23	56.	L1-5		K6-10
3.	C9-1		L1-2	30.	G5-3		G4-13	57.	L12-4		H12-1
4.	C8-1		L1-4	31.	G5-3		L12-15	58.	L12-3		C1-2
5.	C3-8		D1-3	32.	H3-1		L10-6	59.	L12-14		G5-3 (PAD)
6.	C3-10		C3-11	33.	H3-1		H3-15	60.	M10-1		M10-10
7.	D9A-6		C7B-2	34.	H3-11		H5-13	61.	M10-3		C5-6
8.	D1-1		D4-6	35.	H3-12		J12-3	62.	M10-11		L11-12
9.	D3-2		D4-4	36.	H3-13		H5-4	63.	M10-12		K12-13
10.	D3-2		C3-9	37.	H3-14		J12-11	64.	M10-13		G11-13
11.	D4-4		F1-2	38.	J3-1		J3-8	65.	M8-6		K10-13
12.	E7B-2		F9A-6	39.	J3-12		J4-13	66.	M12-1		L13-1
13.	E7A-1		D9A-6	40.	J4-11		J4-10	67.	M12-3		L13-8
14.	E5-6		C5-5	41.	J4-8		F2-15	68.	M12-6		M13-9
15.	E13-10		E13-11	42.	J3-2		PIN 42	69.	M12-10		R57 (POINT C)
16	E1-1		D6-14	43.	J3-3		HJ2-40	70.	M12-11		M14-6
17.	E1-2		E1-5	44.	J3-9		HJ2-20	71.	M12-14		M14-12
18.	F1-4		R28-2	45.	J3-10		HJ2-25	72.	M13-8		M9-3
19.	F2-13		G2-16	46.	K1-10		E1-3	73.	M12-12		EQP-7
20.	F1-2		F1-14	47.	K1-10		K1-1	74.	M12-13		EQP-6
21.	F1-14		F1-13	48.	K1-2		K1-9	75.	R3-2		R15 (POINT D)
22.	F1-5		R22 (POINT B)	49.	K1-3		K1-11	76.	R23 (POINT E)		F1-2
23.	F1-8		F1-10	50.	K1-4		K1-12	77.	R18-1		R9 (POINT F)
24.	F1-8		CR3 CATHODE	51.	K1-6		K8-2	78.	R18-3		R19 (POINT G)
25.	G8-1		E8-1	52.	K1-8		K8-1	79.	R18-2		R14 (POINT H)
26.	G9-1		L1-12	53.	K11-10		M10-9	80.	R28-1		R25 (POINT J)
27.	G8-1	TO	L1-10	54.	L1-5	TO	K8-3	81.	R1 (POINT K)		BC2-24
										TO	

C.

82. D4-7 TO D4-5
83. L11-7 ↕ EQP-E
84. Z10-1 ↕ C11-16
85. F2-20 TO F2-17
86. C73 FROM M13-8 TO GND
87. C74 FROM M9-13 TO GND

REV	ECO	DESCR	DR	DATE	CHK	APPD
01	0518914	PC B. PER ECO	P.P.	6-15-79		AW

THIS DRAWING REPLACES REV 02 CHANGES



F/N	REFERENCE DESIGNATIONS
46	CR1
49	CR2, CR3
72	Z2, Z3, Z8, Z10, Z15, Z16
54	Z17 - Z21
75	Z4 - Z7, Z9, Z11 - Z14
32	R36
33	R11
34	R25, R53
35	R21 - R24
36	R1, R30, R37, R52
37	R28, R29, R31, R32
38	R9, R19, R34, R50, R56, R57, R62, R63
39	R2-5, R20, R33, R35, R39 - R43, R45 - R48, R51, R54, R55, R58, R59, R60, R64, R36
55	R12, R16, R18
41	R15
42	R8, R14, R17
43	R13
44	R27
30	R6, R7, R10
48	C21, C22
58	C16, C24, C75
65	C15, C17, C29, C26, C25, C34, C35, C38, C39, C41 - C44, C46, C49, C51, C53, C56, C57, C59, C61, C62, C67, C70, C71
69	C30 - C33, C58, C63 - C66, C68, C69
70	C18, C19, C20, C23, C25, C27, C28, C36, C37, C40, C45, C47, C48, C50, C52, C54, C55, C60
60	C72, C73

Present Shell Board!

4 INSTALL F/N 52 AFTER WIRE ADDS ARE MADE PER DETACHED NOTES.

3 REMOVE & DISCARD UNUSED SWITCH MOUNTING HARDWARE BEFORE INSTALLING F/N 31.

2 WHEN PWA IS SOLD AS A SPARE, FFP 96751080, MUST ACCOMPANY PWA.

1. ASSEMBLE PER CDC SPEC 88818000.

NOTES: UNLESS OTHERWISE SPECIFIED

PL 96751078 DETACHED LISTS

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES 1 PLACE ± 2 PLACE ± ANGLES ±

DO NOT SCALE DRAWING

MATERIAL

FINISH

CONTRACT

DES	CYBER 19	
DR	B. JOHNSON	1/19/79
ENG	G. LAGE	1/25/79
ENGR	C. LEE	3/1/79
MFG	R. WILKINSON	3/27/79
APPD	A. WEHE	3/1/79

TITLE: PW ASSY — AUTO-RESTART LOADER (7FNT)

CODE IDENT NO	DRAWING NUMBER
09132	96751078

SIZE D | SCALE 1:1 | SHEET 1 OF 1

DWN	[redacted]	2/1/78	CONTROL DATA
CHKD	[redacted]	3-1-78	
ENG	[redacted]	3-2-78	DATA SYSTEMS LAJOLLA DIVISION
MFG	[redacted]	[redacted]	
APPR	[redacted]	3-2-78	CODE IDENT 09132

TITLE PW ASSY - AUTO-RESTART LOADER (7FNT)

PREFIX PL

DOCUMENT NO. 96751078

REV. 01

FIRST USED ON CYBER 18

SHEET 1 OF 4

SHEET REVISION STATUS

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
-1		CLASS C	BA	6-13-78	AW
01	DS18914	CL. B. PRE-RELEASED	BR	6-13-78	AW

Make changes to P/L per "Red" markups.
J. Whitaker

OCT 12 1978

NOTES:

DETACHED LISTS

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

S = SPARE PARTS
N = NON SPARE PARTS

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER
96751078	01	CLB	D	PWA-AUTO-RESTART LOADER 7FNT	DS	CRR 18	06/10/78	06/10/78	1/ 3

MF

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PN NC	S OR N
1	A	15126600	100	PC	I.C. M-QUAD COMPAR. DIP LM339	IN					N
25	A	15128200	1800	PC	I.C. 75453	IN					N
2	A	15144900	400	PC	IC TTL QUAD 2-IN NAND 74LS00	IN			PPP4		N
3	A	15145000	200	PC	IC TTL QUAD 2-INPUT NOR 74LS02	IN			PPP4		N
4	A	15145100	800	PC	IC TTL HEX INVERTER 74LS04	IN			PPP4		N
5	A	15145300	100	PC	IC TTL HEX INVERTER 74LS05	IN			PPP4		N
6	A	15145400	200	PC	IC TTL QUAD 2INPUT AND 74LS08	IN			PPP4		N
7	A	15145600	200	PC	IC TTL TRPL 3INPUT NAND 74LS10	IN			PPP4		N
8	A	15145700	200	PC	I.C. 74LS11	IN					N
9	A	15145900	200	PC	IC TTL DUAL 4INPUT NAND 74LS20	IN			PPP4		N
10	A	15146100	100	PC	I.C. 74L530 74LS30	IN					N
11	A	15146200	300	PC	IC TTL QUAD 2INPUT OR 74LS32	IN			PPP4		N
12	A	15146300	1200	PC	IC TTL DUAL D-TYPE F/F 74LS74	IN			PPP4		N
13	A	15146400	1000	PC	IC TTL QUAD 2INPUT EXC 74LS86	IN			PPP4		N
14	A	15146600	200	PC	IC-74LS139 DECODER TTL DUAL	IN			PPP4		N
15	A	15146900	1200	PC	IC-TTL,LATCH 4 BIT 74LS175	IN			PPP4		N
16	A	15147000	400	PC	IC COUNTER TTL 4-BIT 74LS193	IN			PPP4		N
17	A	15147200	100	PC	IC-74LS85 TTL 4 BIT COMPARATOR	IN			PPP4		N
18	A	15147300	400	PC	IC-MUX DUAL 4-IN TRI 74LS253	IN			PPP4		N
19	A	15147400	100	PC	IC, DECODER-STTL 74LS138	IN			PPP4		N
20	A	15147500	2300	PC	IC LATCH-STTL 6-BIT D-TYPE	IN			PPP4		N
21	A	15151600	200	PC	I.C. 8111A	IN			PPP4		N
22	A	15155300	200	PC	IC-8216 4 BIT BI-DIR BUS DRVR	IN			PPP4		N
23	A	15155400	100	PC	IC-8212 8 BIT I/O PORT	IN			PPP4		N
24	A	15156300	100	PC	IC-8214 PRIORITY INTERRUPT CNT	IN			PPP4		N
26	A	15163201	100	PC	IC Z80A MOS 8 BIT CPU	IN			PPP4		N
27	A	15163224	100	PC	TRANSISTOR ARRAY-PNP HIGH CUR	IN			PPP4		N
28	A	15164427	100	PC	IC-8255A	IN			PPP4		N
30	C	17705936 12	300	PC	RES FXD .25W .100 MEG OHMS	IN			PPP4		N
31	C	18696001	100	PC	SWITCH TOGGLE	IN			PPP4		N
32	C	24500024	1400	PC	RES FXD .25W 24 OHMS	IN			PPP4		N
33	C	24500036	100	PC	RES FXD .25W 75 OHMS	IN			PPP4		N
34	C	24500043	200	PC	RES FXD .25W 150 OHMS	IN			PPP4		N
35	C	24500054	400	PC	RES FXD .25W 430 OHMS	IN			PPP4		N
36	C	24500055	4200	PC	RES FXD .25W 470 OHMS	IN			PPP4		N
37	C	24500065	400	PC	RES FXD .25W 1200 OHMS	IN			PPP4		N

PROJECT ENGINEER
C LEE

SCMD

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

S = SPARE PARTS
N = NON SPARE PARTS

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER
96751078	01	CLB	D	PWA-AUTO-RESTART LOADER 7FNT	DS	CBR 18	06/10/78	06/10/78	2/ 3

MF

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PN NC	S OR N
38	C	24500070	8 00	PC	RES FXD .25W 2000 OHMS	IN			PPP4		N
39	C	24500079	24 27 00	PC	RES FXD .25W 4700 OHMS	IN			PPP4		N
41	C	24500083	1 00	PC	RES FXD .25W 6800 OHMS	IN			PPP4		N
42	C	24500087	3 00	PC	RES FXD .25W 10000 OHMS	IN			PPP4		N
43	C	24500089	1 00	PC	RES FXD .25W 12000 OHMS	IN			PPP4		N
44	C	24500091	1 00	PC	RES FXD .25W 15000	IN			PPP4		N
46	C	24503804	1 00	PC	DIODE SILICON, ZENER	IN			PPP4		N
DELETE → 47	C	24503805	1 00	PC	DIODE SILICON,ZENER	IN			PPP4		N
48	C	24505229	2 00	PC	CAP,FXD SOL TA 35V 1.0UF 10PCT	IN			PPP4		N
49	A	25175800	2 1 00	PC	DIODE(1N914)	IN			PPP4		N
50	A	36186501	11 00	PC	IC CHIP TYPE 1489	IN			PPP4		N
51	A	38838005	1 00	PC	TERM,TUR-SUBMIN,TIN DIP .062	IN			PPP4		N
52	A	39396502	1 00	PC	SWITCH, LOW PROFILE DIP-SPST 4	IN			PPP4		N
54	A	39452200	5 00	PC	RES NETWORK-VOLTAGE DIVIDR-SIP	IN			PPP4		N
55	A	39772108	3 00	PC	POT-CERMET .5W 3/8 SQ 5K OHM	IN			PPP4		N
56	A	50241800	9 00	PC	DIODE ARRAY, 8, DIC16	IN					N
57	A	75009934	2 00	PC	RES PKG-THK FILM,4.7K OHMS	IN			PPP4		N
58	A	84996725	3 2 00	PC	CAP,CER 100V 680 PF	IN			PPP4		N
59	A	88812400	8 00	PC	RIVET-SEMI-TUBULAR,BRS .312 LG	IN			PPP4		N
60	A	88880500	2 00	PC	CAP-FIXED AL,16VDC,100UF	IN			PPP4		N
61	A	88881000	1 00	PC	IC-TR1602A (UART) MOS DATA I/F	IN			PPP4		N
62	A	88896000	12 00	PC	IC 8123 TTL TRI-STATE 2-IN MUX	IN			PPP4		N
63	A	88897800	25 00	PC	CAP-FIXED SOLID TANT,6VDC,12UF	IN			PPP4		N
64	A	88918800	12 11 00	PC	IC 8T97 TTL TRI-STATE HEX BFR	IN			PPP4		N
65	A	88920800	6 00	PC	IC 74S258 TTL QUAD 1-L SEL/MUX	IN			PPP4		N
66	A	88920900	3 4 00	PC	IC 8T98 TTL TRI-ST HEX BFR/INV	IN			PPP4		N
67	A	88924500	2 00	PC	IC 7404 TTL HEX INVERTER	IN			PPP4		N
68	A	88945400	7 4 00	PC	JUMPER 24AWG TEF INSULATED .50	IN			PPM4		N
69	A	89636100	11 00	PC	CAP,FXD CER 270PF	IN			PPP4		N
70	A	89636157	18 00	PC	CAP,FXD CER .1 MFD 50 VDCW	IN			PPP4		N
72	A	91938552	6 00	PC	RESISTOR MODULE 8 PIN	IN			PPP4		N
73	C	39396501	1 00	PC	SWITCH, LOW PROFILE DIP-SPST 8 SEG	IN			PPP4		N
74	C	94260302	3 00	PC	SOCKET I.C.	IN					N
75	A	94375103	9 00	PC	RES NETWORK, 8PIN SIP 470 OHMS	IN			PPP4		N
76	A	96744154	5 00	PC	IC 7403 TTL QUAD 2-IN POS NAND	IN			PPP4		N
77	D	96751077	1 00	PC	PWB-AUTO-RESTART LOADER	IN			PPP4		N

PROJECT ENGINEER: C LEE

SCMD

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

S = SPARE PARTS
N = NON SPARE PARTS

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER
96751078	01	CLB	D	PWA-AUTO-RESTART LOADER 7FNT	DS	CBR 18	06/10/78	06/10/78	3/ 3

MF

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE BUY PART TYPE	PN NC	S OR N
78	C	96751079	REF	PC	LOGIC-AUTO-RESTART LOADER 7FNT	IN			RFE4		N
79	C	96752479	2.00	PC	INSULATOR-CARD FRAME	IN			PYP4		N
80	C	96752480	1.00	PC	FRAME-CARD (MODIFIED)	IN			PYP4		N
81	A	51903807	2.00	PC	INDICATOR-LED	IN			PPP4		N
82	A	96754700	1.00	PC	IC-8K ROM, AUTO RESTART, LOC. A3	IN					N
83	A	96860401	1.00	PC	OSCILLATOR-HRD CLK, 16.0000 MHZ	IN			PPP4		N
84	A	88882800	1.00	PC	IC - TTL 74174 LATCH 6-BIT						
85		51858103	2.00	PC	SOCKET, IC 40 PIN						

ADD

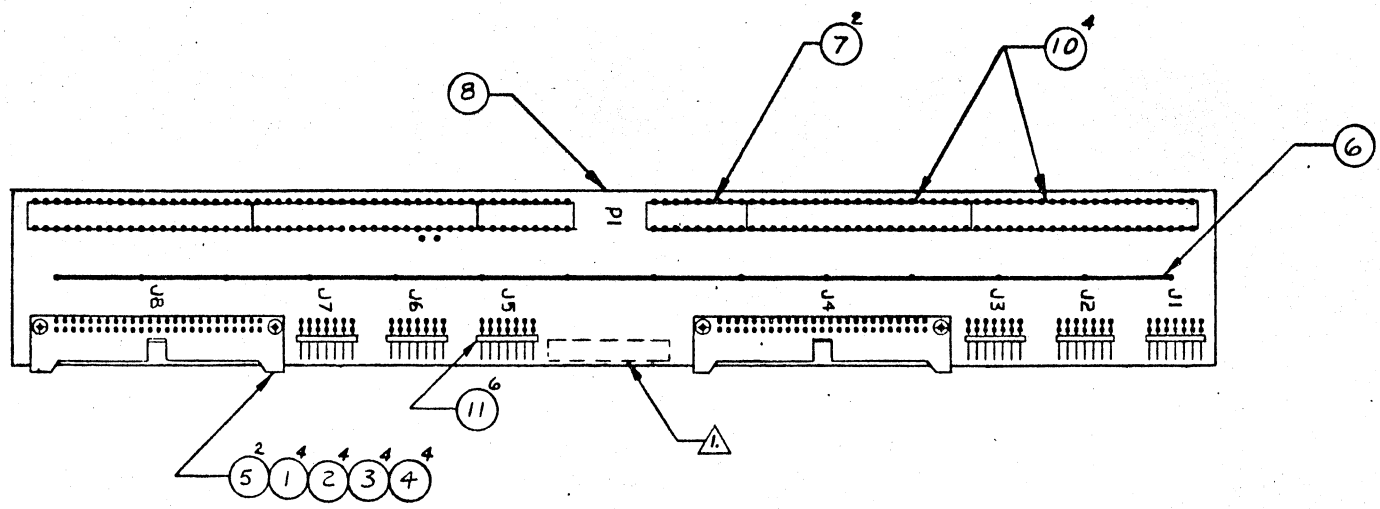
NUMBER OF LINE ITEMS = 78
HIGHEST FIND NUMBER = 83

PROJECT ENGINEER: C LEE

SCMD

AA 2709-1 REV. 7-75

REVISION RECORD						
REV	ECO	DESCRIPTION	DFT	DATE	CHK	APPD
-1		CLASS C	B.H.	3-14-78	TF	MC
01	D518914	CL B. PRE-RELEASED	JM	4-25-78	TF	AM



3. COMPONENT SIDE VIEWED. (SIDE 2)
2. WHEN PWA IS SOLD AS SPARE, FPP 96752622 MUST ACCOMPANY PWA.
1. IDENTIFY WITH PART NO. PER CDC STD 1-01-009.

NOTES: UNLESS OTHERWISE SPECIFIED

PL 96752620 DETACHED LISTS

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
1 PLACE ± / 2 PLACE ± / ANGLES ± /
DO NOT SCALE DRAWING
MATERIAL
FINISH

CONTROL DATA SYSTEMS LA JOLLA DIVISION LA JOLLA, CA 92037

NEXT USED ON	1855-1	
DR	B. Hall	3-30-78
CHK	T. Cynthia	4-13-78
ENGR	C. Lee	4-14-78
MFG		
APPD		4-14-78

TITLE
PWA - AUTO RESTART LOADER
PADDLE BOARD
8HLT

	CODE IDENT NO.	DRAWING NUMBER
C	09132	96752620

SCALE 1/1 | 96752643 | SHEET 1 OF 1

96752620

3

DWN	[illegible]	3-30-78	GD DATA SYSTEMS LAJOLLA DIVISION	TITLE PWA - AUTO RESTART LOADER PADDLE BOARD	PREFIX	DOCUMENT NO. / REV.
CHKD	T. Cyrulnik	4-13-78			PL	96752620 / 01
ENG	C. Lee	4-14-78		FIRST USED ON 1855-1 (8HLT)		SHEET 1 OF 2
MFG			CODE IDENT 09132			
APPR	A. Wolk	6-15-78				

SHEET REVISION STATUS

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
-1		CLASS C	BH	4-14-78	TG	[illegible]
01	DS18914	CL. B. PRE-RELEASED	JM	6-15-78	[illegible]	AW

NOTES:

DETACHED LISTS

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

S = SPARE PART
N = NON SPARE PARTS

SH 2

MF

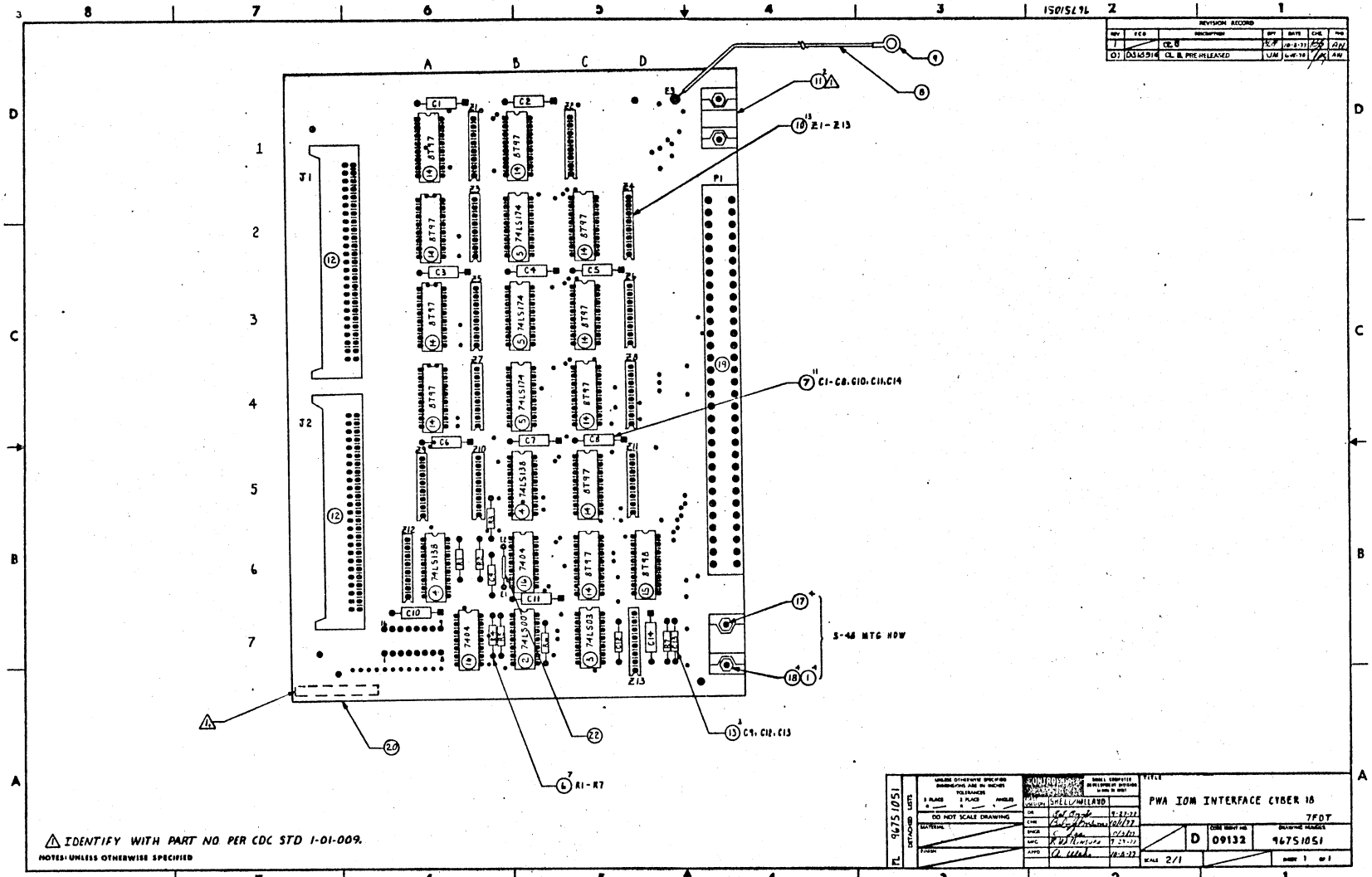
ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER
96752620	01	CLB	C	PWA-ARL PADDLE BOARD 8HLT	DS	FV679A	06/10/78	06/10/78	~~1/1~~

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PN NC	S OR N
1	A	10125102	400	PC	HEXAGON MACHINE SCREW NUTS	IN			PPP1		N
2	A	10125602	400	PC	PLAIN WASHERS	IN			PPP1		N
3	A	10125800	400	PC	SPRING LOCK WASHERS (MED.)	IN			PPP1		N
4	A	10127170	400	PC	SCR MACH PAN PHL 2-56	IN			PPP1		N
5	A	39903606	200	PC	CONN,HEADER,RIGHT ANGLE (2X25)	IN			PPP4		N
6	D	88875500	100	PC	BUS BAR (13 IN)	IN			PPP4		N
7	A	96751917	200	PC	CONNECTOR-PWB .125 CTR 18 POS	IN			PPP4		N
8	C	96752619	100	PC	PWB-ARL PADDLE BOARD	IN					N
9	C	96752621	REF	PC	SCHEM DIAG-ARL PADDLE BD 8HLT	IN					N
10	A	96756701	400	PC	CONNECTOR-PWB .125 CENTERS	IN			PPP4		N
11	A	96756705	600	PC	CONN-HEADER,RIGHT ANGLE (2X7)	IN					N

NUMBER OF LINE ITEMS = 11
HIGHEST FIND NUMBER = 11

PROJECT ENGINEER
C LEE

SCMD


ISO15L96
REVISION RECORD
REV
ECO
DESCRIPTION
BY
DATE
CHK
APP
01
D3165914
CL & PRE-RELEASED
UM
11-14-78
AM
J1
J2
P1
C1
C2
C3
C4
C5
C6
C7
C8
C9
C10
C11
C12
C13
C14
8T97
74LS174
74LS138
7404
74LS00
74LS03
8T96
8T17
(9)
(8)
(11) 2
(10) 13 Z1 - Z13
(7) 11 C1 - C8, C10, C11, C14
(17)
(18) 1
5-48 MTG HDW
(13) 3 C9, C12, C13
(22)
(6) 7 R1 - R7
(20)
1 IDENTIFY WITH PART NO PER CDC STD 1-01-009.
NOTES: UNLESS OTHERWISE SPECIFIED
DO NOT SCALE DRAWING
SHELL/MILLARD
TITLE
PWA IOM INTERFACE CYBER 18
7FDT
D
09132
9675 1051
SCALE 2/1
9675 1051
DETACHED LISTS

DWN	[illegible]	8-22-77
CHKD	[illegible]	10/4/77
ENG	C. Lee	10/3/77
MFG	[illegible]	[illegible]
APPR	[illegible]	10-3-77

CONTROL DATA
DATA SYSTEMS LAJOLLA DIVISION
CODE IDENT 09132

TITLE: PWA-IOM INTERFACE-CYBER 18

PREFIX	DOCUMENT NO.	REV.
PL	96751051	01

FIRST USED ON: SHELL/HOLLAND

SHEET 1 OF 2

SHEET REVISION STATUS

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
1		CL B	PEP	10-3-77	AW
01	DS18914	CL. B. PRE-RELEASED	JM	6-15-78	AW

NOTES:

DETACHED LISTS

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

S = SPARE PART
N = NON SPARE PARTS

SH 2

MF

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER
96751051	01	CLR	D	PWA-IOM INTERFACE 7FDT	DS	DN134A	06/10/78	06/10/78	~~1~~ 1

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PN NC	S OR N
1	A	10125800	400	PC	SPRING LOCK WASHERS (MED.)	IN			PPP1		N
2	A	15144900	100	PC	IC TTL QUAD 2-IN NAND 74LS00	IN			PPP4		N
3	A	15145200	100	PC	IC TTL QUAD 2INPUT NAND 74LS03	IN			PPP4		N
4	A	15147400	200	PC	IC, DECODER-STTL 74LS138	IN			PPP4		N
5	A	15147500	300	PC	IC LATCH-STTL 6-BIT D-TYPE	IN			PPP4		N
6	C	24500070	700	PC	RES FXD .25W 2000 OHMS	IN			PPP4		N
7	C	24505229	1100	PC	CAP,FXD SOL TA 35V 1.0UF 10PCT	IN			PPP4		N
8	C	25195020	1200	IN	WIRE TEF INSUL 18AWG WHITE	IN			PPP3		N
9	A	25198806	100	PC	TERM,RING 16-22AWG NO. 8 STUD	IN			PPP4		N
10	A	39452200	1300	PC	RES NETWORK-VOLTAGE DIVIDR-SIP	IN			PPP4		N
11	C	39827500	200	PC	GUIDE,APPROACH	IN			PPP4		N
12	A	39903606	200	PC	CONN,HEADER,RIGHT ANGLE (2X25)	IN			PPP4		N
13	A	84996725	300	PC	CAP,CER 100V 680 PF	IN			PPP4		N
14	A	88918800	1000	PC	IC 8T97 TTL TRI-STATE HEX BFR	IN			PPP4		N
15	A	88920900	100	PC	IC 8T98 TTL TRI-ST HEX BFR/INV	IN			PPP4		N
16	A	88924500	200	PC	IC 7404 TTL HEX INVERTER	IN			PPP4		N
22	A	88945400	100	PC	JUMPER 24AWG TEF INSULATED .50	IN			PPM4		N
17	A	92742046	400	PC	SCREW,MACH PAN HEAD 3-48	IN			PPP4		N
18	A	93014003	400	PC	HEX NUT 3-48	IN			PPP4		N
19	C	94243400	100	PC	CONNECTOR-CARD MTG 62 SOCKET	IN			PPP4		N
20	C	96751050	100	PC	PWB-IOM INTERFACE	IN					N
21	C	96751052	REF	PC	LOGIC DIAG-IOM INTERFACE 7FDT	IN					N

NUMBER OF LINE ITEMS = 22
HIGHEST FIND NUMBER = 22

PROJECT ENGINEER
C LEE

SCMD

3

TABULATION		
PART NO.	LG/FT	TOL ±
96754881	25	1 FT
96754882	5	8 IN.

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
01	DS18914	CL. B. PRE-RELEASED	JM	6-13-78	[illegible]	AW

△6 TYPE ON CONN LABEL (F/N 6) AT "B" END INFO AS SHOWN.

△5 TYPE ON CONN LABED (F/N 6) AT "A" END INFO AS SHOWN.

4. UNUSED WIRES TO BE TRIMMED AND LEFT UNTERMINATED.

△3 PLUG EXTRA CONTACTS (F/N 10) IN CAVITIES 11, 13, and 14.

2. ASSENBLY OF F/N 9 TO BE DETERMINED AT INSTALLATION.

1. IDENTIFY CABLE PER ES38876000.

DSGN	D. McKay	5-5-78
CHKD	[illegible]	6-13-78
ENG	C Lee	6-8-6
MFG		
APP	[illegible]	6-13-78

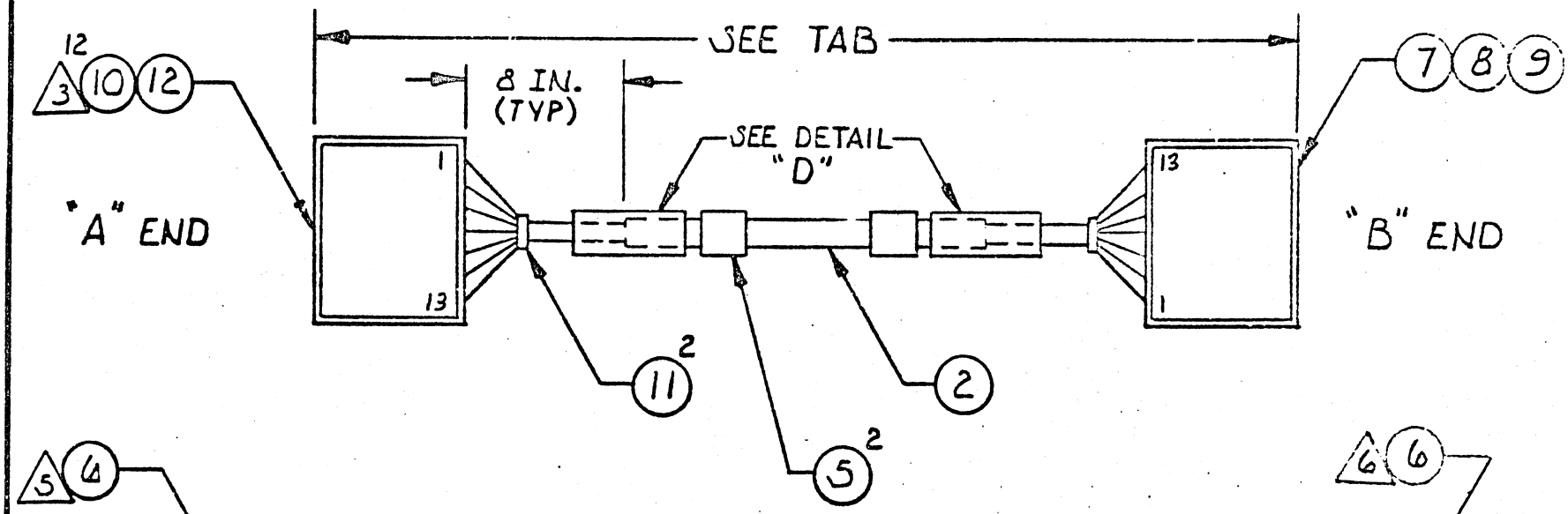
DATA SYSTEMS
LA JOLLA DIVISION
LA JOLLA CA. 92137

TITLE CABLE ASSY-STALL ALARM PANEL (14 PIN TO 25 PIN CONN)

CODE IDENT 09132 | A | DWG NO 96754881/85

SCALE | 96752848 | SHEET 1 OF 6

DATA SYSTEMS LA JOLLA DIVISION LA JOLLA, CA. 92037	CODE IDENT 09132	SHEET	DOCUMENT NO 967548B1-B5	F 01



CDC LJLOPS
967548XX
PROJ NO. PART NO.
ARL
STALL PANEL

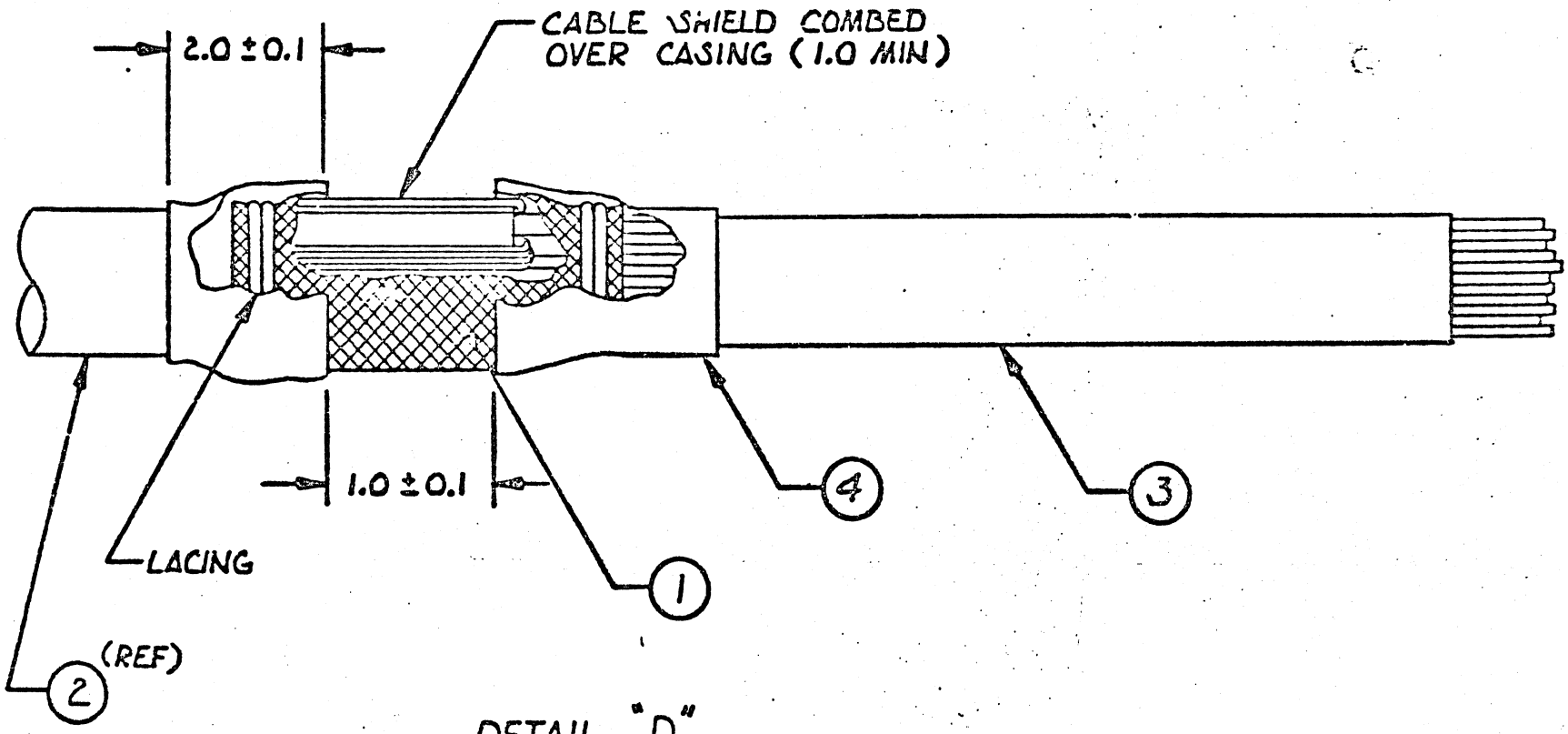
WIRING END-"A"

LABEL- F/N 5
(REF)

WIRING END-"B"

AA3185

	DATA SYSTEMS LA JOLLA DIVISION LA JOLLA, CA. 92037	CODE IDENT 09132	SHEET 3		DOCUMENT NO 96754881/85	REV 01



DETAIL "D"
(NO SCALE)

	DATA SYSTEMS LA JOLLA DIVISION LA JOLLA, CA 92037	CODE IDENT 09132	SHEET 4	WL	DOCUMENT NO. 96754881-85	REV. 01

CONDUCTOR IDENT.	FIND NO.	GAUGE (REF.)	COLOR (REF.)	LENGTH (APPROX)	ORIGIN		ACCESS FIND NO.	DESTINATION		ACCESS FIND NO.	REMARKS
1	2	24	BLK	TAB	B END	1		A END	12	10	GND
2			RED			2			8		REL #1
3			YEL			3			7		REL #2
4			GRN			4			6		AUDALM
5			BLU			5			5		STLLITE
6			WHT BLK			6			1		STLOFF/
7			WHT BRN			7			4		RESET
8			WHT RED			10			3		FLDSTL
9	2	24	WHT ORN	TAB	B END	11		A END	2	10	+5V

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

SH 5

MF

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER
96754882	01	CLB	A	CABLE ASSY-STALL ALARM PNL 5FT	DS	CBR 18	06/10/78	06/10/78	1/1

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PN NC	S OR N
1	C	24534811	300	IN	SHIELD FLECT BRAIDED-BULK	IN			PPP1		N
2	C	24546701	6000	IN	CABLE 24 CONDUCTOR 24 AWG U/L	IN					N
3	A	25196921	1000	IN	INSUL SLEEVE SHRINK 1/2 BLACK	IN			PPP3		N
4	A	25196922	800	IN	INSUL SLEEVE SHRINK 3/4 BLACK	IN			PPP3		N
5	B	39296400	200	PC	LABEL, CABLE MARKING	IN			PPP4		N
6	A	39397104	200	PC	LABEL,WRITE ON	IN			PPP4		N
7	C	93609008	100	PC	CONN, MINI,25 CONT,RECEPTACLE	IN			PPP4		N
8	C	93609013	100	PC	CONN, MINI25 CONT, CABLE HSG,	IN			PPP4		N
9	C	93609016	100	PC	CONN, MINI ALL SIZES LATCH	IN			PPP4		N
10	C	94245600	1200	PC	CONTACT-CRIMP,INSERT,SOCKET	IN			PPP3		N
11	C	94277411	200	PC	STRAP,CABLE TIE TYPE I 5,50 LG	IN			PPP4		N
12	C	94361107	100	PC	HOUSING CONN .100 14 CAVITY	IN			PPP4		N

NUMBER OF LINE ITEMS = 12
HIGHEST FIND NUMBER = 12

PROJECT ENGINEER: C LEE

SCMD

CONTROL DATA CORPORATION

ASSEMB PARTS LIST

S = SPARE PARTS
N = NON SPARE PARTS

MF

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER
96754881	01	CLB	A	CABLE ASSY-STALL ALA PNL 25FT	DS	XA241A	06/10/78	06/10/78	1-1-1

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PN NC	S OR N
1	C	24534811	300	IN	SHIELD ELECT BRAIDED-BULK	IN			PPP1		N
2	C	24546701	30000	IN	CABLE 24 CONDUCTOR 24 AWG U/L	IN					N
3	A	25196921	1000	IN	INSUL SLEEVE SHRINK 1/2 BLACK	IN			PPP3		N
4	A	25196922	800	IN	INSUL SLEEVE SHRINK 3/4 BLACK	IN			PPP3		N
5	B	39296400	200	PC	LABEL, CABLE MARKING	IN			PPP4		N
6	A	39397104	200	PC	LABEL, WRITE ON	IN			PPP4		N
7	C	93609008	100	PC	CONN, MINI, 25 CONT, RECEPTACLE	IN			PPP4		N
8	C	93609013	100	PC	CONN, MINI25 CONT, CABLE HSG,	IN			PPP4		N
9	C	93609016	100	PC	CONN, MINI ALL SIZES LATCH	IN			PPP4		N
10	C	94245600	1200	PC	CONTACT-CRIMP, INSERT, SOCKET	IN			PPP3		N
11	C	94277411	200	PC	STRAP, CABLE TIE TYPE I 5.50 LG	IN			PPP4		N
12	C	94361107	100	PC	HOUSING CONN .100 14 CAVITY	IN			PPP4		N

NUMBER OF LINE ITEMS = 12
HIGHEST FIND NUMBER = 12

PROJECT ENGINEER
C LEE

SCMD

AA 2709-1 REV 7-75

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
01	DS18914	CL. B. PRE-RELEASED	JM	6-13-78	[illegible]	AH

3 TYPE ON CONN LABEL (F/N 6) AT "P01/P02" END INFO AS SHOWN.

2 TYPE ON CONN LABEL (F/N 6) AT "A" END INFO AS SHOWN.

1. IDENTIFY CABLE PER ES 38876000.

NOTES: UNLESS OTHERWISE SPECIFIED.

DWN	[illegible]	5-3-78
CHKD	[illegible]	6-5-78
ENG	C. Lee	6-8-78
MFG		
APP	[illegible]	6-13-78

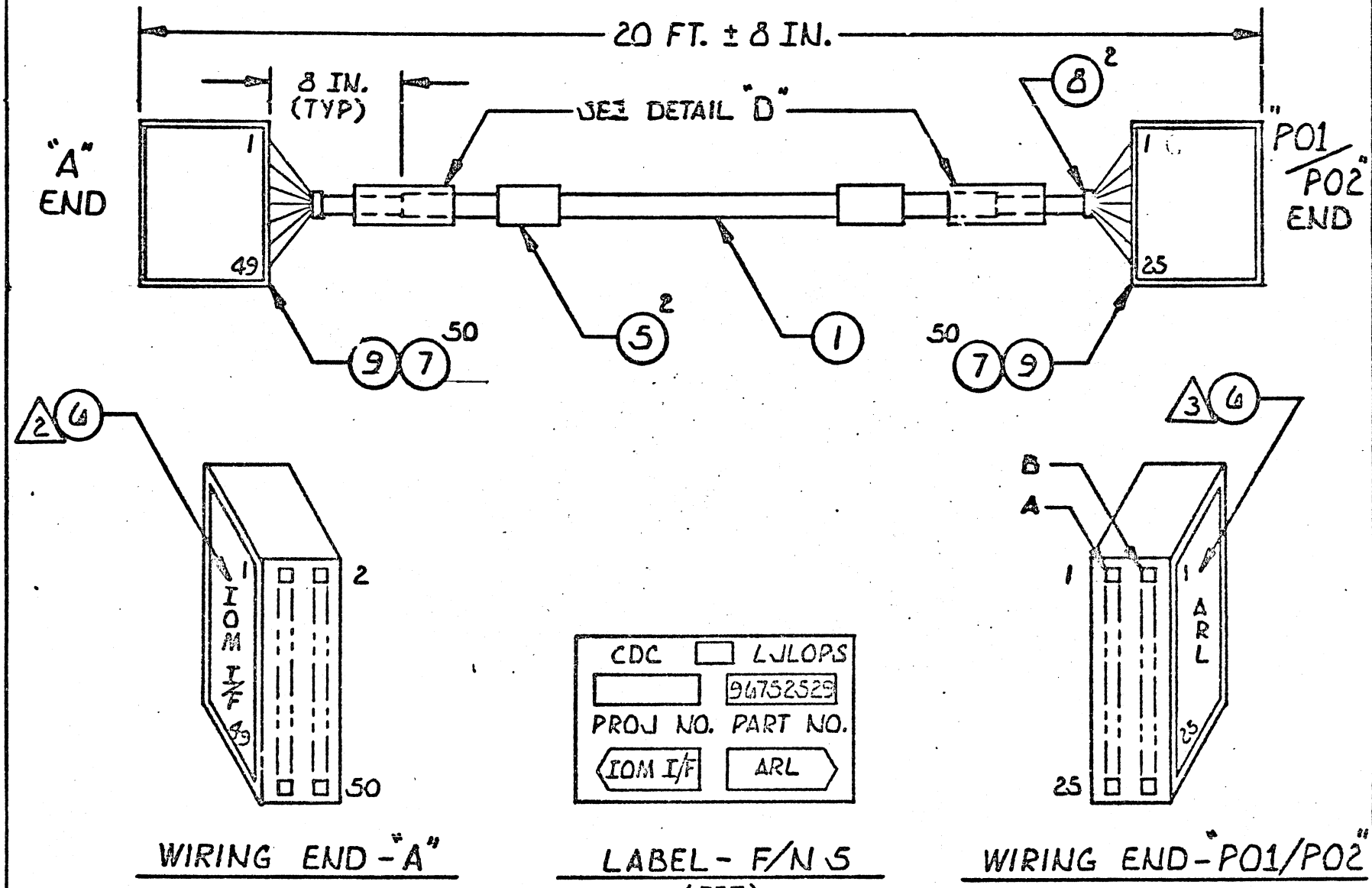
DATA SYSTEMS
LA JOLLA DIVISION
LA JOLLA CA 92037

TITLE CABLE ASSY - IOM INTERFACE (50 PIN TO 50 PIN CONN)

CODE IDENT 09132 | SIZE A | DWG No 96752529

SCALE | 96754878 | SHEET 1 OF 7

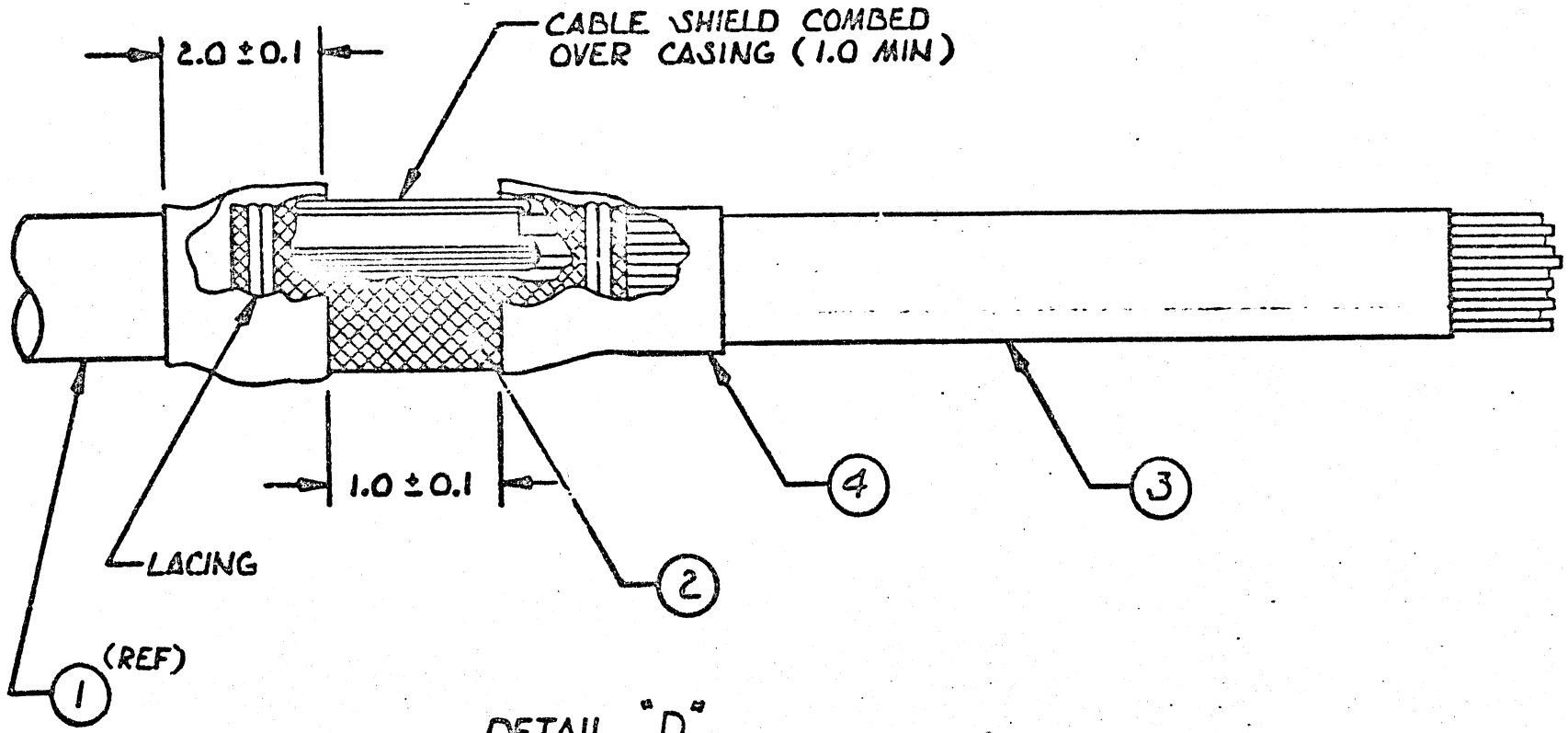
DATA SYSTEMS LA JOLLA DIVISION LA JOLLA, CA. 92037	CODE IDENT 09132	SHEET 2		DOCUMENT NO. 94752529	REV. 01



WIRING END - "A"

LABEL - F/N 5
(REF)

WIRING END - "P01/P02"



DETAIL "D"
(NO SCALE)

	DATA SYSTEMS LA JOLLA DIVISION LA JOLLA, CA 92037	CODE IDENT 09132	SHEET 4	WL	DOCUMENT NO 96752529	REV 01

CONDUCTOR IDENT	FIND NO.	GAUGE (REF.)	COLOR (REF.)	LENGTH (APPROX)	ORIGIN		ACCESS FIND NO.	DESTINATION		ACCESS FIND NO	REMARKS
1	1	24	BLK	20'	A END	1	7	P01/P02	A1	7	TW PR (TYP)
2			WHT			2			B1		GND
3			RED			3			A2		
4			WHT			4			B2		
5			YEL			5			A3		
6			WHT			6			B3		
7			GRN			7			A4		
8			WHT			8			B4		
9			BLU			9			A5		
10			WHT			10			B5		
11			WHT BLK			11			A6		
12			WHT			12			B6		
13			WHT BRN			13			A7		
14			WHT			14			B7		
15			WHT RED			15			A8		
16			WHT			16			B8		
17			WHT ORN			17			A9		
18			WHT			18			B9		
19			WHT YEL			19			A10		
20	1	24	WHT	20'	A END	20	7	P01/P02	B10	7	

	DATA SYSTEMS LA JOLLA DIVISION LA JOLLA, CA 92037	CODE IDENT 09132	SHEET 5	WL	DOCUMENT NO. 94752529	REV 01

CONDUCTOR IDENT.	FIND NO.	GAUGE (REF.)	COLOR (REF.)	LENGTH (APPROX)	ORIGIN		ACCESS FIND NO.	DESTINATION		ACCESS FIND NO.	REMARKS
21	1	24	WHT GRN	20'	A END	21	7	P01/P02	A11	7	TW PR (TYP)
22	↓	↓	WHT	↓	↓	22	↓	↓	B11	↓	GND
23			WHT BLU			23			A12		
24			WHT			24			B12		
25			WHT VIO			25			A13		
26			WHT			26			B13		
27			WHT GRY			27			A14		
28			WHT			28			B14		
29			WHT BLK BLK			29			A15		
30			WHT			30			B15		
31			WHT BRN BLK			31			A16		
32			WHT			32			B16		
33			WHT RED BLK			33			A17		
34			WHT			34			B17		
35			WHT ORN BLK			35			A18		
36			WHT			36			B18		
37			WHT YEL BLK			37			A19		
38			WHT			38			B19		
39	↓	↓	WHT GRN BLK	↓	↓	39	↓	↓	A20	↓	
40	1	24	WHT	20'	A END	40	7	P01/P02	B20	7	

DATA SYSTEMS LA JOLLA DIVISION LA JOLLA, CA 92037	CODE IDENT 09132	SHEET 6	WL	DOCUMENT NO 96752529	REV 01

CONDUCTOR IDENT.	FIND NO.	GAUGE (REF.)	COLOR (REF.)	LENGTH (APPROX)	ORIGIN		ACCESS FIND NO.	DESTINATION		ACCESS FIND NO.	REMARKS
41	1	24	WHT BLU BLK	20'	A END	41	7	P01/P02	A21	7	TW PR (TYP)
42			WHT			42			B21		GND
43			WHT VIO BLK			43			A22		
44			WHT			44			B22		
45			WHT GRY BLK			45			A23		
46			WHT			46			B23		
47			WHT NONE BLK			47			A24		
48	1	24	WHT	20'	A END	48	7	P01/P02	B24	7	

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AA3183 REV. 8 71

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE P
N = NON SPA
PARTS

SH 7

MF

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER
96752529	01	CLB	A	CABLE ASSY-IOM INTERFACE 20FT	DS	DN134A	06/10/78	06/10/78	1/1

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PN NC	S OR N
1	C	24518001	24000	IN	CABLE ELEC 24 TWISTED PR	IN			PPP4		N
2	C	24534A11	300	IN	SHIELD ELECT BRAIDED-BULK	IN			PPP1		N
3	A	25196921	1000	IN	INSUL SLEEVE SHRINK 1/2 BLACK	IN			PPP3		N
4	A	25196922	800	IN	INSUL SLEEVE SHRINK 3/4 BLACK	IN			PPP3		N
5	B	39296400	200	PC	LABEL, CABLE MARKING	IN			PPP4		N
6	A	39397100	200	PC	LABEL, WRITE ON	IN			PPP4		N
7	C	94245600	10000	PC	CONTACT-CRIMP, INSERT, SOCKET	IN			PPP3		N
8	C	94277411	200	PC	STRAP, CABLE TIE TYPE I 5.50 LG	IN			PPP4		N
9	C	94361116	200	PC	HOUSING CONN .100 50 CAVITY	IN			PPP4		N

NUMBER OF LINE ITEMS = 9
HIGHEST FIND NUMBER = 9

PROJECT ENGINEER
C LEE

SCMD

AA 2709-1 REV 7-75

APPENDIX A

CRRTMS 2.0

CRTARL AUTO RESTART LOADER

PROGRAM DESCRIPTION

CRTARL TEST PROCEDURE

```
MI
CONTROL WORD, PGM NAME
START, TSTARL    (CR)
BEGIN 1855-1 AUTO RESTART LOADER TEST
1855-1 INT LINE, WES CODE
2, 0    (CR)  *
TEST, SECTION MSGS {0=NO, 1=YES}
E   (CR)
TSTARL DIO PARAMETERS
SECTS, RUNS
1E, XXXX    (CR)
USER PATTERN 1, PATTERN 2
XXXX, XXXX    (CR)
TSTARL STL PARAMETERS
SECTS, RUNS
6, X    (CR)
TSTARL CTL BEGIN TEST
TSTARL CTL END TEST XXXX RUNS 0000 ERRORS
TSTARL DIO BEGIN TEST
TSTARL STL BEGIN TEST
TSTARL DIO END TEST XXXX RUNS 0000 ERRORS
TSTARL STL END TEST XXXX RUNS 0000 ERRORS
```

```
0002          NAM  CRTARL      DECK-ID R[illegible]  CRRTMS 2.0          SUMMARY-132  R3800001
0003          *    CRRTMS TEST ROUTINE FOR 1855-1 AUTORESTART LOADER (XA216)         R3800002
0003          *    DATA SYSTEMS - LA JOLLA DIVISION                                  R3800003
0004          *    COPYRIGHT CONTROL DATA CORPORATION 1978                           R3800004

0006          ********************************************************************** R3800006
0007          *                                                                      *R3800007
0008          *                        PROGRAM DESCRIPTION                           *R3800008
0009          *                                                                      *R3800009
0010          ********************************************************************** R3800010

0012          *    CRTARL IS A DIAGNOSTIC FOR THE 1855-1 AUTORESTART LOADER          R3800012
0013          *    WHICH RUNS UNDER THE CONTROL OF THE CRRTMS SUPERVISOR/MONITOR.    R3800013
0014          *    IT TEST ALL THE FEATURES OF LOADER WITH EXCEPTION OF THE PROM     R3800014
0015          *    LOADER. THE FEATURES TESTED ARE:                                  R3800015
0016          *                                                                      R3800016
0017          *        - A/Q CONTROL FOR AUTORESTART LOADER.                         R3800017
0018          *        - PROGRAMMABLE DIGITAL INPUT/OUTPUT UNIT.                     R3800018
0019          *        - STALL ALARM AND PANEL                                       R3800019
0020          *        - A/Q EXPANSION FOR STANDARD IOM INTERFACING.                 R3800020
0021          *                                                                      R3800021
0022          *    EACH FEATURE IS TESTED BY A SEPARATE AND INDEPENDENT TEST.        R3800022
0023          *    THE LAST THREE FEATURES CAN BE TESTED CONCURRENTLY. THERE ARE     R3800023
0024          *    SEVERAL RESTRICTIONS ON THE TEST EXECUTION, THEY ARE AS FOL-      R3800024
0025          *    LOWS:                                                             R3800025
0026          *                                                                      R3800026
0027          *        - IF ONLY THE A/Q CONTROL TEST IS SELECTED, IT WILL CAUSE     R3800027
0028          *          ALL OTHER TESTS TO STOP EXECUTING AS CONTROL IS NEVER       R3800028
0029          *          RELEASED EXCEPT WHEN MESSAGES ARE PRINTED.                  R3800029
0030          *        - IF ANY OTHER TEST IS SELECTED ALONG WITH A/Q CONTROL        R3800030
0031          *          TEST, THE A/Q CONTROL TEST WILL BE EXECUTED ONLY ONCE.      R3800031
0032          *        - WHEN THE A/Q EXPANSION TEST IS RUN, NO CHECK IS MADE FOR    R3800032
0033          *          OTHER TESTS BEING RUN ON IOM SUBSYSTEM; THEREFORE ERRORS    R3800033
0034          *          CAN BE CAUSED IN OTHER TESTS.                               R3800034
0035          *                                                                      R3800035
0036          *    THE FOLLOWING IS A FUNCTIONAL DESCRIPTION OF EACH TEST SECTION.   R3800036
0037          *                                                                      R3800037
0038          *    TEST 1 -- A/Q CONTROL TEST                                        R3800038
0039          *                                                                      R3800039
0040          *      A. INPUT UNIT STATUS, CHECK FOR REJECTS.                        R3800040
0041          *      B. OUTPUT UNIT FUNCTION, CHECK FOR REJECTS.                     R3800041
0042          *      C. OUTPUT DIGITAL FUNCTION = ZERO, CHECK FOR REJECTS.           R3800042
0043          *      D. CHECK ALL MODULE ADDRESSES FOR PROPER I/O RESPONSE.          R3800043
0044          *                                                                      R3800044
0045          *          STATION     WRITE                READ                       R3800045
0046          *          NUMBER      OPERATION            OPERATION                  R3800046
0047          *          ------      ---------            ---------                  R3800047
0048          *            00        REPLY                REPLY                      R3800048
0049          *            01        REPLY                INTERNAL REJECT            R3800049
0050          *            02        REPLY                INTERNAL REJECT            R3800050
0051          *            03        REPLY                REPLY                      R3800051
```

04	EXTERNAL REJECT	INTERNAL REJECT	P3800052
05	EXTERNAL REJECT	INTERNAL REJECT	P3800053
06	EXTERNAL REJECT	INTERNAL REJECT	P3800054
07	EXTERNAL REJECT	INTERNAL REJECT	P3800055
08	NOT TESTED	INTERNAL REJECT	P3800056
09 TO 0F	INTERNAL REJECT	INTERNAL REJECT	P3800057

P3800058

E. CHECK REMAINING REPLY/REJECT MODES OF DIGITAL I/O UNIT. P3800059

P3800060

DIGITAL FUNCTION	STATION NUMBER	WRITE OPERATION	READ OPERATION	
00F0	04	REPLY	INTERNAL REJECT	P3800064
00F0	05	REPLY	INTERNAL REJECT	P3800065
00F0	06	REPLY	INTERNAL REJECT	P3800066
00F0	07	REPLY	INTERNAL REJECT	P3800067
000F	04	INTERNAL REJECT	EXTERNAL REJECT	P3800068
000F	05	INTERNAL REJECT	EXTERNAL REJECT	P3800069
000F	06	INTERNAL REJECT	EXTERNAL REJECT	P3800070
000F	07	INTERNAL REJECT	EXTERNAL REJECT	P3800071
00FF	04	INTERNAL REJECT	REPLY	P3800072
00FF	05	INTERNAL REJECT	REPLY	P3800073
00FF	06	INTERNAL REJECT	REPLY	P3800074
00FF	07	INTERNAL REJECT	REPLY	P3800075
50F0	04	INTERNAL REJECT	INTERNAL REJECT	P3800076
50F0	05	REPLY	INTERNAL REJECT	P3800077
50F0	06	INTERNAL REJECT	INTERNAL REJECT	P3800078
50F0	07	REPLY	INTERNAL REJECT	P3800079
50FF	04	INTERNAL REJECT	INTERNAL REJECT	P3800080
50FF	05	INTERNAL REJECT	REPLY	P3800081
50FF	06	INTERNAL REJECT	INTERNAL REJECT	P3800082
50FF	07	INTERNAL REJECT	REPLY	P3800083

P3800084

F. CHECK REPLY/EXTERNAL REJECT TIMES ON SUCCESSIVE COMMANDS ON THE SAME STATION NUMBERS. P3800085 P3800086

G. CHECK FOR REPLY ON SUCCESSIVE COMMANDS ON DIFFERENT STATION NUMBERS. P3800087 P3800088

P3800089

NOTE: WHEN THIS TEST IS SELECTED ALONG WITH OTHER TESTS, IT IS ONLY EXECUTED ONE TIME. THE USER IS NOT REQUESTED TO ENTER NUMBER OF RUNS. IF AN ERROR IS DETECTED DURING THE PASS THRU THIS SECTION THE TEST IS TERMIANTED WITHOUT GOING ON TO OTHER REQUESTED TESTS. P3800090 P3800091 P3800092 P3800093 P3800094 P3800095

P3800096

TEST 2 -- DIGITAL INPUT/OUTPUT UNIT TEST (SECTION 1). P3800097

P3800098

A. SET DIGITAL UNIT IN WORD AND TEST MODE. P3800099

B. OUTPUT $FFFF TO WORD ZERO, $0000 TO WORD ONE. P3800100

C. INPUT EACH WORD AND VERIFY DATA. P3800101

D. OUTPUT $0000 TO WROD ZERO, $FFFF TO WORD ONE. P3800102

E. INPUT EACH WORD AND VERIFY DATA. P3800103

F. SET BYTES 0 THRU 3 INVERTED. P3800104

```
0105    *      G. REPEAT STEPS B THRU F.                                    R3800105
0106    *                                                                   R3800106
0107    *   TEST 2 -- DIGITAL INPUT/OUTPUT UNIT TEST (SECTION 2).           R3800107
0108    *                                                                   R3800108
0109    *      A. SET DIGITAL UNIT IN WORD AND TEST MODE.                   R3800109
0110    *      B. OUTPUT $0000 TO WORD ZERO, SHIFT A ONE BIT THRU WORD ONE  R3800110
0111    *         VERIFYING DATA ON EACH WORD AFTER EACH SHIFT.              R3800111
0112    *      C. OUTPUT $0000 TO WORD ONE, SHIFT A ONE BIT THRU WORD ZERO  R3800112
0113    *         VERIFYING DATA ON EACH WORD AFTER EACH SHIFT.              R3800113
0114    *                                                                   R3800114
0115    *   TEST 2 -- DIGITAL INPUT/OUTPUT UNIT TEST (SECTION 3).           R3800115
0116    *                                                                   R3800116
0117    *      A. SET DIGITAL UNIT IN WORD AND TEST MODE.                   R3800117
0118    *      B. OUTPUT $FFFF TO WORD ZERO, SHIFT A ZERO BIT THRU WORD ONE R3800118
0119    *         VERIFYING DATA ON EACH WORD AFTER EACH SHIFT.              R3800119
0120    *      C. OUTPUT $FFFF TO WROD ONE, SHIFT A ZERO BIT THRU WORD ZERO R3800120
0121    *         VERIFYING DATA ON EACH WORD AFTER EACH SHIFT.              R3800121
0122    *                                                                   R3800122
0123    *   TEST 2 -- DIGITAL INPUT/OUTPUT UNIT TEST (SECTION 4).           R3800123
0124    *                                                                   R3800124
0125    *      A. SET DIGITAL UNIT IN WORD AND TEST MODE.                   R3800125
0126    *      B. OUTPUT USER VALUE 1 TO WORD ZERO, USER VALUE 2 TO WORD ONE. R3800126
0127    *      C. INPUT EACH WORD AND VERIFY DATA.                          R3800127
0128    *      D. OUTPUT USER VALUE 1 TO WORD ONE, USER VALUE 2 TO WORD ZERO. R3800128
0129    *      E. INPUT EACH WORD AND VERIFY DATA.                          R3800129
0130    *      F. SET BYTES 0 THRU 3 INVERTED.                              R3800130
0131    *      G. REPEAT STEPS B THRU E.                                    R3800131
0132    *                                                                   R3800132
0133    *   TEST 2 -- DIGITAL INPUT/OUTPUT UNIT TEST (SECTION 5).           R3800133
0134    *                                                                   R3800134
0135    *      A. REQUIRES SPECIAL TEST CABLE TO BE INSTALLED.              R3800135
0136    *      B. SET BYTE 0 AND 1 OUTPUT, BYTE 2 AND 3 INPUT.              R3800136
0137    *      C. SHIFT A ONE BIT THRU AND VERIFY DATA.                     R3800137
0138    *      D. SHIFT A ZERO BIT THRU AND VERIFY DATA.                    R3800138
0139    *      E. SET BYTES 0 THRU 3 INVERTED.                              R3800139
0140    *      F. REPEAT STEPS C AND D.                                     R3800140
0141    *      G. SET BYTE 0 AND 1 INPUT, BYTE 2 AND 3 OUTPUT.              R3800141
0142    *      H. REPEAT STEPS C THRU F.                                    R3800142
0143    *                                                                   R3800143
0144    *   TEST 2 -- DIGITAL INPUT/OUTPUT UNIT TEST (SECTION 6).           R3800144
0145    *                                                                   R3800145
0146    *      A. REQUIRES SPECIAL TEST CABLE TO BE INSTALLED.              R3800146
0147    *      B. SET BYTE 0 AND 1 OUTPUT, BYTE 2 AND 3 INPUT.              R3800147
0148    *      C. SET IN SYNC MODE.                                         R3800148
0149    *      D. CHECK REJECT CONDITIONS.                                  R3800149
0150    *      E. SET SYNCS.                                                R3800150
0151    *      F. CHECK REJECT CONDITIONS.                                  R3800151
0152    *      G. CHECK FOR INTERRUPT CONDITIONS.                           R3800152
0153    *      H. SET RESPONSE.                                             R3800153
0154    *      I. CHECK FOR INTERRUPT CONDITIONS.                           R3800154
0155    *      J. CHECK REJECT CONDITIONS.                                  R3800155
0156    *      K. SET BYTE 0 AND 1 INPUT, BYTE 2 AND 3 OUTPUT.              R3800156
0157    *      L. REPEAT STEPS C THRU J.                                    R3800157
```

```
0158  *                                                              R3800158
0159  *      TEST 3 -- STALL ALARM UNIT T--(SECTION 1).              R3800159
0160  *                                                              R3800160
0161  *        A. OUTPUT ALL MEANING FUNCTION COMBINATIONS.           R3800161
0162  *        B. READ STATUS AFTER EACH OUTPUT AND COMPARE TO EXPECTED VALUE.R3800162
0163  *        C. LOAD AND RESET COUNTERS.                           R3800163
0164  *        D. CHECK OVERFLOW STATUS.                             R3800164
0165  *        E. CHECK INTERRUPT ON OVERFLOW.                       R3800165
0166  *                                                              R3800166
0167  *      TEST 3 -- STALL ALARM UNIT TEST (SECTION 2).            R3800167
0168  *                                                              R3800168
0169  *        A. USING MAXIMUM TIME VALUE FOR COUNTER 1 (256 MSEC) VERIFY  R3800169
0170  *           NO STALL CONDITION WHEN RESET EVERY 250 MILLISEC AND      R3800170
0171  *           STALL CONDITION OCCURS WHEN RESET IS ATTEMPTED EVERY      R3800171
0172  *           267 MILLISEC.                                      R3800172
0173  *        B. USING MAXIMUM TIME VALUE FOR COUNTER 2 (25.6 SEC) VERIFY  R3800173
0174  *           NO STALL CONDITION WHEN RESET EVERY 25.5 SECONDS AND      R3800174
0175  *           STALL CONDITION OCCURS WHEN RESET IS ATTEMPTED EVERY      R3800175
0176  *           25.7 SECONDS.                                      R3800176
0177  *                                                              R3800177
0178  *           NOTE: THE CYBER 18 CPU CLOCK OR THE 1572-1 SAMPLE TIMING  R3800178
0179  *                 UNIT WILL BE USED AS THE TIMING BASE. ONE OF THESE  R3800179
0180  *                 UNITS MUST BE DECLARED AS THE SYSTEM TIMER. A       R3800180
0181  *                 CHECK WILL BE MADE TO INSURE THAT TIMER INTERRUPTS   R3800181
0182  *                 ARE OCCURRING BUT IF THE TIME BASE IS INCORRECT     R3800182
0183  *                 ERRORS WILL OCCUR IN THIS TEST.                     R3800183
0184  *                                                              R3800184
0185  *      TEST 3 -- STALL ALARM UNIT TEST (SECTION 3).            R3800185
0186  *                                                              R3800186
0187  *        A. REQUEST USER TO SET FIELD STALL.                   R3800187
0188  *        B. WAIT FOR STALL INTERRUPT FOR 30 SECONDS.           R3800188
0189  *        C. CHECK STATUS.                                      R3800189
0190  *        D. REQUEST USER TO CLEAR FIELD STALL.                 R3800190
0191  *        E. CHECK STATUS.                                      R3800191
0192  *                                                              R3800192
0193  *      TEST 4 -- A/Q EXPANSION TEST - REQUIRES IOM ADAPT.(1855-200) R3800193
0194  *                                                              R3800194
0195  *        A. SET A/Q TEST MODE.                                 R3800195
0196  *        B. OUTPUT AND INPUT TO ALL POSSIBLE MODULE AND SLOT   R3800196
0197  *           ADDRESSES ($00 TO $FF), DATA EQUALS WEMS CODE.     R3800197
0198  *        C. OUTPUT AND INPUT SHIFTING ONE BIT PATTERN.         R3800198
0199  *        D. OUTPUT AND INPUT SHIFTING ZERO BIT PATTERN.        R3800199
0200  *        E. OUTPUT AND INPUT ALTERNATING $FFFF AND $0000 PATTERNS.  R3800200
0201  *        F. OUTPUT AND INPUT ALTERNATING $AAAA AND $5555 PATTERNS.  R3800201
0202  *        G. CLEAR A/Q TEST MODE                                R3800202
0203  *                                                              R3800203
0204  *           NOTE: WHEN THIS TEST IS SELECTED NO CHECKS ARE MADE FOR   R3800204
0205  *                 OTHER IOM TESTS EXECUTING OVER THE A/Q EXPANSION.    R3800205
0206  *                 THEREFORE THIS TEST WHILE EXECUTING WILL CAUSE      R3800206
0207  *                 ERRONOUS ERROR CONDITIONS TO OCCUR IN THOSE TESTS.  R3800207
0208  *                                                              R3800208
0209  *    DURING THE EXECUTION OF ALL TEST SECTIONS. ANY ABNORMAL,  R3800209
0210  *    UNEXPECTED OR ERRONOUS CONDITIONS ARE REPORTED VIA A MESSAGE  R3800210
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PROM

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0001                    NAM  PROM          18840100 190678 STPM/MFEI                          PRM00001
0002                *I 18840100 190678 PROM    'PROM PROG CYBER 18 RESTARTLOADER'  NDS      PRM00002
0003                *R 18840100 190678 PROM    'ORIGINAL RELEASE. NO PWF TEST   '  NDS      PRM00003
0004                *B                                                                        PRM00004
0005                *       PROGRAM FUNCTIONS:                                                PRM00005
0006                *                                                                         PRM00006
0007                *       1) MASTER CLEAR                                                   PRM00007
0008                *       2) CLEAR CPU REGISTERS AND FILES                                  PRM00008
0009                *       3) CLEAR MEMORY LOCATIONS WHERE PROM WILL BE LOADED (LOC. $0C00)  PRM00009
0010                *       4) LOAD PROM PROGRAM AND START EXECUTION                          PRM00010
0011                *       5) DO CHECKSUM CHECK ON LOADED PROGRAM                            PRM00011
0012                *       6) CLEAR REMAINDER OF 65K MEMORY, STARTING AT LOCATION $0100      PRM00012
0013                *       7) SET PROTECT BITS IN LOWER 65K OF MEMORY                        PRM00013
0014                *          NOTE: PROGRAM SPACE WRITES DATA AND SETS PROTECT BITS          PRM00014
0015                *                IN EXTENDED MEMORY                                       PRM00015
0016                *       8) READ SYSTEM DISK NUMBER FROM DIGITAL INPUT BYTE 0              PRM00016
0017                *          READ AUTOLOAD SECTORS FROM THIS DISK  to $1100                 PRM00017
0018                *       9) START EXECUTION OF AUTOLOAD PROGRAM.                           PRM00018
0019                *                                                                         PRM00019
0020                *E                                                                        PRM00020
0021                *                                                                         PRM00021
0022                *                                                                         PRM00022
0023                PCC     MAC  P1           PANEL CONTROL COMMAND                           PRM00023
0024                        ALF  *,'P1'*                                                      PRM00024
0025                        EMC                                                               PRM00025
0026                *                                                                         PRM00026
0027                        ENT  PROMST       FIRST AND LAST ADDRESS                          PRM00027
0028                        ENT  PROMND       FOR CHECKSUM GENERATION.                        PRM00028

0030        0002            EQU  LPMSK(2)                                                     PRM00030
0031        0012            EQU  RPMSK($12)                                                   PRM00031
0032        0078            EQU  NSEC(120)    DISKS ARE READY 'NSEC' SECONDS AFTER POWER ON.  PRM00032
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0034 P0000 3F1B   MC      NUM  $3F1B          MASTER CLEAR, ESCAPE TO PANEL MODE          PRM00034
0035                      PCC  K21008000:     SET FCR, SELECT K, P                        PRM00035
0035 P0001 4B32
     P0002 3130
     P0003 3038
     P0004 3030
     P0005 303A
0036                      PCC  L00:           K = 0                                       PRM00036
0036 P0006 4C30
     P0007 303A
0037                      PCC  J06:           SELECT F1                                   PRM00037
0037 P0008 4A30
     P0009 363A
0038                      PCC  L000           CLEAR F1                                    PRM00038
0038 P000A 4C30
     P000B 3030
0039 P000C 80FF           NUM  $80FF                  (256 LOCATIONS)                     PRM00039
0040              *                                                                       PRM00040
0041                      PCC  K0C00:         SET P = $0C00 (START ADDRESS FOR PROM PROG)  PRM00041
0041 P000D 4B30
     P000E 4330
     P000F 303A
0042                      PCC  J07:           SELECT MEMORY                               PRM00042
0042 P0010 4A30
     P0011 373A
0043                      PCC  L000           CLEAR MEMORY AREA FOR PROM                  PRM00043
0043 P0012 4C30
     P0013 3030
0044 P0014 8104           ADC  (PROML)                (PROML + 1 LOCATIONS)               PRM00044
0045              *                                                                       PRM00045
0046                      PCC  K0C00:         SET P = $0C00                               PRM00046
0046 P0015 4B30
     P0016 4330
     P0017 303A
0047 P0018 4CBC           NUM  $4CBC          L $BC  START LOADING OF PROM PROGRAM        PRM00047
0048              *                                FROM PROM ADDRESS AS SET BY JUMPERS.   PRM00048
0049              *                                ( = ADDRESS OF LABEL PAJUMP) =60       PRM00049
0050         0003 P       EQU  P1(*/8)                                                    PRM00050
0051         0020 P       EQU  P2S(P1*8+8)    LET NEXT CODING START AT A                  PRM00051
0052 P0019 0007           BZS  (P2S-*)        PROM ADDRESS WHICH IS MULTIPLE OF 16        PRM00052

0054         0020  WASPPS EQU  WASPPS(*-MC)       = WORD ADDRESS SET PPS CODE            PRM00054
0055         0041  PASPPS EQU  PASPPS(2*WASPPS+1) = PROM (BYTE) ADDRESS                  PRM00055
0056               *                                                                     PRM00056
0057 P0020 001B   SETPPS NUM  $001B           ESCAPE TO PANEL MODE                        PRM00057
0058                      PCC  J48:           SUPPRES CONSOLE TRANSMIT                    PRM00058
0058 P0021 4A34
     P0022 383A
0059                      PCC  J28:           SET PROGRAM PROTECT SWITCH                  PRM00059
0059 P0023 4A32
     P0024 383A
0060                      PCC  J04:           SELECT Q-REG                                PRM00060
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0060 P0025 4A30
     P0026 343A
0061                    PCC  L0000:        CLEAR Q TO INDICATE PROGRAM PROTECT SWITCH SETPRM00061
0061 P0027 4C30
     P0028 3030
     P0029 303A
0062                    PCC  J40@          ENABLE CONSOLE TRANSMIT                      PRM00062
0062 P002A 4A34
     P002B 3040
0063 P002C BB00         NUM  $BB00         TERMINATE LOADING                            PRM00063

0065       0005 P       EQU  P2(*/8)                                                    PRM00065
0066       0030 P       EQU  P3S(P2*8+8)                                                PRM00066
0067 P002D 0003         BZS  (P3S-*)                                                    PRM00067
0068                 *                                                                  PRM00068
0069       0030   WAJUMP EQU  WAJUMP(*-MC)                                             PRM00069
0070       0060   PAJUMP EQU  PAJUMP(2*WAJUMP)                                         PRM00070
0071 P0030 A207         ADC  ($2000+PROML*2-1)  TRANSFER 2*PROML BYTES WITH BINARY DATA PRM00071
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0073        0031 P PROMST EQU  PROMST(*)                                  PRM00073


0075 P0031 E000    PROM   LDQ  =XPROML-1    DO CHECKSUM CHECK             PRM00075
     P0032 0103
0076 P0033 0844           CLR  A                                          PRM00076
0077 P0034 BAFC           EOR* PROM,Q                                     PRM00077
0078                      DQP  1                                          PRM00078
0078 P0035 06A1
0079 P0036 0102           SAZ  OK           SKIP IF CHECKSUM OK           PRM00079
0080 P0037 0C00           ENQ  0                                          PRM00080
0081 P0038 18FF    CKSERR NUM  $18FF        HANG IF CHECKSUM ERROR        PRM00081


0083 P0039 5801    OK     RTJ* HERE                                       PRM00083
0084 P003A 0000    HERE   NUM  0                                          PRM00084
0085 P003B C838           LDA* AFWA$100                                   PRM00085
0086 P003C 682E    CLEAR  STA* PWFFLG       PWFFLG = 0 IF POWER FAILURE, ELSE $0100  PRM00086
0087 P003D 0862           TCA  Q                                          PRM00087
0088 P003E F8FB           ADQ* HERE          CLEAR MEMORY FROM LOCATION   PRM00088
0089 P003F 0DF5           INQ  PROM-HERE-1   $0000 OR $0100 - START OF PROM PROGRAM  PRM00089
0090 P0040 0844           CLR  A                                          PRM00090
0091 P0041 6E29    CLRLP1 STA* (PWFFLG),Q                                 PRM00091
0092                      DQP  *-CLRLP1                                   PRM00092
0092 P0042 06A1
0093               *                                                      PRM00093
0094 P0043 0C01           ENQ  1             CLEAR MEMORY FROM END OF PROGRAM  PRM00094
0095 P0044 4C27           STQ* (ZERO)        THROUGH LOCATION $FFFF       PRM00095
0096 P0045 6A00    CLRLP2 STA  PROMND,Q      TERMINATE WHEN LOC $0000 HAS BEEN CLEARED  PRM00096
     P0046 00EE
0097 P0047 0D01           INQ  1                                          PRM00097
0098                      SFZ* (ZERO),15,16                               PRM00098
0098 P0048 05C2
0098 P0049 FF22
0099 P004A 18FA           JMP* CLRLP2                                     PRM00099
0100 P004B 6C21           STA* (HFFFF)                                    PRM00100
0101               *                                                      PRM00101
0102               *                  SET PROTECT BITS                    PRM00102
0103 P004C 0802           SET  Q           IN LOWER 65K MEMORY           PRM00103
0104 P004D 0600    SETPB  SPB  0                                          PRM00104
0105 P004E 0142           SQZ  2                                          PRM00105
0106 P004F 0DFE           INQ  -1                                         PRM00106
0107 P0050 18FC           JMP* SETPB                                      PRM00107
0108 P0051 01C0           SPE  0           CLEAR POSSIBLE PARITY ERROR    PRM00108
0109               *                                                      PRM00109
0110 P0052 C818           LDA* PWFFLG                                     PRM00110
0111 P0053 0118           SAN  NOTPWF      SKIP IF NOT POWER FAILURE      PRM00111
0112 P0054 E000           LDQ  =X20*NSEC                                  PRM00112
     P0055 0960
0113 P0056 C000    DELLP  LDA  =N22520      EXECUTION                      PRM00113
     P0057 57F8
0114                      DAP  0           TIME IS                        PRM00114
0114 P0058 06C0
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0115                    DQP   *-DELLP       APPROX. 50 MILLI SECONDS                    PRM00115
0115 P0059 06A3
0116 P005A 0844         CLR   A                                                         PRM00116
0117 P005B 1808         JMP*  RDDSK                                                     PRM00117
0118               *                                                                    PRM00118
0119 P005C E000   NOTPWF LDQ   =N$0004      READ DIGITAL                              PRM00119
     P005D 0004
0120 P005E 0844         CLR   A             INPUT BYTE 0.                             PRM00120
0121 P005F 0201         INP   1                                                       PRM00121
0122 P0060 0B00         NOP   0                                                       PRM00122
0123 P0061 A000         AND   =N7           EXTRACT UNIT NUMBER OF                    PRM00123
     P0062 0007
0124 P0063 0908   RDDSK INA   8             SYSTEM DISK  (INCLUDING 'REVERSE' BIT)    PRM00124
0125 P0064 0FC4         ALS   4             AND STORE IN                              PRM00125
0126 P0065 680A         STA*  AUNTSL        UNIT SELECT CODE.                         PRM00126
0127               *                                                                  PRM00127
0128 P0066 585D         RTJ*  QMASS         READ AUTOLOAD SECTORS.                    PRM00128
0129               *                                                                  PRM00129
0130 P0067 0C06         ENQ   6             AUTO RESTART PROM                         PRM00130
0131 P0068 C807         LDA*  AUNTSL        GO EXECUTE                                PRM00131
0132 P0069 1C0A         JMP*  (AFWA)        AUTOLOAD PROGRAM.                         PRM00132
0133               *                                                                  PRM00133
0134 P006A 0100   PWFFLG NUM  $0100                                                   PRM00134
0135 P006B 0000   ZERO   NUM  0                                                       PRM00135
0136 P006C FFFF   HFFFF  NUM  $FFFF                                                   PRM00136
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0138                ****
0139                *       THIS DRIVER PROVIDES SOFTWARE CONTROL OF CARTRIDGE DISK DRIVES-PRM00139
0140                *       THROUG CYEBER-18 CONTROLLER.                                  PRM00140
0141                *                                                                     PRM00141
0142        0002            EQU  DENSTY(2)     DRIVER FOR DOUBLE DENSITY "HAWK" DRIVES   PRM00142
0143                *                                                                     PRM00143
0144                *                                                                     PRM00144
0145                *                ************************************************** PRM00145
0146                *                *       ONLY READ OF AUTO LOAD SECTORS IS DONE     * PRM00146
0147                *                *                                                  * PRM00147
0148                *                *       FWA                = $0100                 * PRM00148
0149                *                *       NUMBER OF WORDS = $0600                    * PRM00149
0150                *                *       SECTOR ADDRESS  = $0000                    * PRM00150
0151                *                *                                                  * PRM00151
0152                *                *       DRIVER RETURNS IF NO ERROR                 * PRM00152
0153                *                *                                                  * PRM00153
0154                *                *       DRIVER HANGS AT LABEL 'DSKERR' IF ERROR    * PRM00154
0155                *                *       Q-REG = ERROR CODE                         * PRM00155
0156                *                *       A-REG = STATUS                             * PRM00156
0157                *                *                                                  * PRM00157
0158                *                *              ERROR CODE'S:                         PRM00158
0159                *                *              2 = ALARM ERROE                     * PRM00159
0160                *                *              5 = INTERNAL REJECT                 * PRM00160
0161                *                *              6 = EXTERNAL REJECT                 * PRM00161
0162                *                *              7 = NO COMPER ERROR                 * PRM00162
0163                *                *             13 = WRITE PROJECT                   * PRM00163
0164                *                *             14 = NOT READY                       * PRM00164
0165                *                *             17 = SEEK ERROR                      * PRM00165
0166                *                *             70 = BUS OFF                         * PRM00166
0167                *                *             74 = SECTOR ADDRESS TOO GREAT        * PRM00167
0168                *                *             FF = UNKNOWN ERROR                   * PRM00168
0169                *                *                                                  * PRM00169
0170                *                ************************************************** PRM00170
0171                *                                                                     PRM00171
0172                *                                                                     PRM00172
0173                *       DESCRIPTION:                                                  PRM00173
0174                *       ------------                                                  PRM00174
0175                *                                                                     PRM00175
0176                *       THIS PROGRAM IS A STATUS DRIVEN DRIVER.THIS MEANS THAT        PRM00176
0177                *       INSTEAD OF USING INTERRUPTS TO SIGNAL THE END OF SPECIFIED    PRM00177
0178                *       OPERATIONS,IT LOOPS ON THE STATUS AND WAITS UNTIL SPECIFIED   PRM00178
0179                *       CONDITIONS ARE MET (EOP,ON CYLINDER,ETC.).                    PRM00179
0180                *       THE DRIVER OPERATION IS BASED ON A TABLE COMPOSED OF          PRM00180
0181                *        7  VECTORS.THE  N-TH  ENTRY IN THIS TABLE  GIVES THE        PRM00181
0182                *       REQUIRED A AND Q REGISTERS FOR THE N-TH OUTPUT OPERATION,     PRM00182
0183                *       TWO MASKS FOR THE STATUS WORD AND THE  EXPECTED RESULTS       PRM00183
0184                *       AFTER APPLYING THESE MASKS,AND POINTERS TO ROUTINES TO BE     PRM00184
0185                *       EXECUTED  AFTER THE OUTPUT OPERATIONS.                        PRM00185
0186                *       THE TABLE ENTRIES ARE ORDERED ACCORDING TO THE SEQUENCE       PRM00186
0187                *       OF INSTRUCTIONS SENT TO THE CONTROLLER.                       PRM00187
0188                *                                                                     PRM00188
0189                *       A TYPICAL I/O CYLCLE IS AS FOLLOWS (DISREGARDING              PRM00189
0190                *       ROUTINES'  BOUNDARIES ) :                                     PRM00190
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0191  *              SET  I-REG. TO ORDINAL NO. OF REQUIRED I/O.                PRM00191
0192  *              NOTE: LOCATION IOINDX IS USED IN STEAD OF I-REG            PRM00192
0193  *                    IN THIS VERSION                                     PRM00193
0194  *              JMP  ACCORDING TO PREVEC ( BY I )                         PRM00194
0195  *              LDA  FROM TABLE (INDEXED BY I-REG.)                       PRM00195
0196  *              LDQ  FROM TABLE (BY I)                                    PRM00196
0197  *              ADQ  EQUIPMENT CODE                                       PRM00197
0198  *              OUT  REJECT - *                                           PRM00198
0199  *              GET  DYNAMIC STATUS  IN A.                                PRM00199
0200  *              AND  WITH WATMSK FROM TABLE (BY I)                        PRM00200
0201  *              EOR  WITH WATRSL  FROM TABLE (BY I)                       PRM00201
0202  *              WAIT UNTIL A=0 (I.E.: IF A #0 THEN GET A NEW STATUS)      PRM00202
0203  *              LDA  WITH LAST STATUS                                     PRM00203
0204  *              AND  WITH ERRMSK (BY I)                                   PRM00204
0205  *              EOR  WITH ERRSLT  (BY I)                                  PRM00205
0206  *              IF A=0 THEN CONTINUE.ELSE - RETURN ERROR.                 PRM00206
0207  *              JMP  ACCORDING TO NEXTBL ( BY I )                         PRM00207
0208  *                                                                        PRM00208
0209  *       WATMSK ENABLES THE DRIVER TO WAIT UNTIL CERTAIN EVENTS HAVE      PRM00209
0210  *       OCCURRED ( EOP,ON CYLINDER ETC.).                                PRM00210
0211  *       ERRMSK CHECKS IF ANY ERROR CONDITION HAS BEEN SET, AND IF SO,    PRM00211
0212  *       IT EXITS FROM THE DRIVER.                                        PRM00212
0213  *                                                                        PRM00213
0214  *                                                                        PRM00214
0215  *       NEXTBL ENABLE THE PROGRAMMER TO SET  PARAMETERS                  PRM00215
0216  *       BEFORE EACH OUTPUT AND TO CHECK CONDITIONS (OR ERRORS )          PRM00216
0217  *       OR  EVEN REPEAT THE OUTPUT AFTER EACH OPERATION.                 PRM00217
0218  *                                                                        PRM00218
0219  *                                                                        PRM00219
0220  *       AFTER THE REQUEST IS FINISHED,THE UNIT IS DESELECTED             PRM00220
0221  *       AND THE BUS IS RELEASED.                                         PRM00221
0222  *                                                                        PRM00222
0223  *                                                                        PRM00223
0224  *       THE STATUS WORD IS BUILT AS FOLLOWS:                             PRM00224
0225  *                                                                        PRM00225
0226  *        15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0                 PRM00226
0227  *       ---------------------------------------------------              PRM00227
0228  *       I  I  I  I  IXXIXXIXXI  I  IXXI  I  I  I  I  I                  PRM00228
0229  *       ---------------------------------------------------              PRM00229
0230  *         '  '  '  '           '  '     '  '  '  '  '  '                PRM00230
0231  *         '  '  '  '           '  '     '  '  '  '  '  '                PRM00231
0232  *         '  '  '  ON BUS      '  SINGLE'  '  '  '  '  UNIT READY(=1)  PRM00232
0233  *         '  '  '              '  DNSITY'  '  '  '  '                   PRM00233
0234  *         '  '  DEVICE SEEK    '  (=1)  '  '  '  '  CONTROLLER BUSY =1 PRM00234
0235  *         '  '  ERROR          '        '  '  '  '                      PRM00235
0236  *         '  '                 EOP(=1)  '  '  '  INTERRUPT            PRM00236
0237  *         '  CONTROLLER                 '  '  '                         PRM00237
0238  *         '  PROTECTED                  '  '  ALARM                     PRM00238
0239  *         '                             '  '                            PRM00239
0240  *        BUS BUSY                       '  ON CYLINDER                  PRM00240
0241  *                                       '                               PRM00241
0242  *                                       DISK WRITE PROTECTED            PRM00242
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0244                *       D R I V E R   S U B R O U T I N E                                    PRM00244
0245                *                                                                           PRM00245


0247                *       THE FOLLOWING IS THE TABLE FOR OUTPUT OPERATIONS.IT CONTAINS         PRM00247
0248                *       7 VECTOR:                                                           PRM00248
0249                *            AVEC - A REG. FOR OUTPUTS                                      PRM00249
0250                *            QVEC - Q REG. FOR OUTPUTS                                      PRM00250
0251                *            WATMSK - MASK FOR WAITING ON STATUS                            PRM00251
0252                *            WATRSL - DESIRED RESULT AFTER APPLYING THE MASK ABOVE.         PRM00252
0253                *            ERRMSK - MASK FOR CHECKING ERRORS AT THE END OF                PRM00253
0254                *                     AN OUTPUT OPERATION                                   PRM00254
0255                *            ERRSLT - THE RESULT OF APPLYING THE MASK ABOVE TO THE          PRM00255
0256                *                     STATUS WORD IF NO ERROR OCCURRED.                     PRM00256
0257                *       NEXTBL - POINTER TO NEXT ROUTINE TO BE EXECUTE                      PRM00257
0258                *                                                                           PRM00258
0259                *       NOTE :                                                              PRM00259
0260                *            THE OPERATION OF THE DRIVER IS BASED ON SEQUENTIAL             PRM00260
0261                *            EXECUTION OF I/O'S ACCORDING TO THIS TABLE.THEREFORE,          PRM00261
0262                *            ADDING A NEW I/O IS DONE BY  ADDING  THE APPROPRIATE           PRM00262
0263                *            ROUTINE  AND  BY ADDING AN ENTRY TO EACH OF THE                PRM00263
0264                *            VECTORS ABOVE IN THE PROPER PLACE ACCORDING TO THE             PRM00264
0265                *            SEQUENCE.                                                      PRM00265
0266                *            EVEN WHEN NO WATMSK OR ERRMSK IS NEEDED - A ZERO ENTRY         PRM00266
0267                *            MUST BE INSERTED IN THE UNNEEDED  VECTORS.                     PRM00267
0268                *                                                                           PRM00268
0269                *       SEEK (AND RTZS) OPERATIONS INCLUDE WAITING FOR "ON CYLINDER"        PRM00269
0270                *       SIGNAL,AND NOT JUST "EOP".                                          PRM00270
0271                *                                                                           PRM00271


0273 P006D 0000   AVEC    BSS   AVEC(0)        A-REG. FOR OUTPUT OPERATIONS                    PRM00273


0275 P006D 0000   ACLCNT  NUM   0               CLEAR CONTROLLER & WAIT FOR BUS NOT BUSY        PRM00275
0276 P006E 0080   ABSCON  NUM   $80              BUS CONNECT                                     PRM00276
0277 P006F 0080   AUNTSL  ADC   UNTSEL          UNIT SELECT; DEFAULT IS UNIT 0                  PRM00277
0278 P0070 0020   ARTZS   NUM   $20              RTZS - RETURN TO ZERO SEEK                      PRM00278
0279 P0071 0000   ABNKSL  NUM   0               MEMORY BANK 0 SELECT                            PRM00279
0280 P0072 0600   ALNGTH  ADC   16*96           REQUESTED BLOCK LENGTH                          PRM00280
0281 P0073 0100   AFWA    NUM   $100            FIRST WORD ADDRESS of Autoload Read             PRM00281
0282 P0074 0000   ASKRW   NUM   0               SEEK FOR READ/WRITE/WRITE TAGS /COMPARE         PRM00282
0283 P0075 0009   ARDWRC  ADC   RDCODE          READ                                            PRM00283
0284 P0076 000B   ACOMP   ADC   CMCODE          COMPARE                                         PRM00284
0285 P0077 0000   AUNTDS  NUM   0               UNIT DESELECT : INSERTED BY PROG.               PRM00285
0286 P0078 0000   ABSREL  NUM   0               BUS RELEASE                                     PRM00286


0288 P0079 0000   QVEC    BSS   QVEC(0)        Q-REG. FOR OUTPUT                               PRM00288
0289 P0079 0010           NUM   $10             CLEAR CONTROLLER & WAIT FOR BUS NOT BUSY        PRM00289
0290 P007A 0008           NUM   $8              BUS CONNECT                                     PRM00290
0291 P007B 0006           NUM   $6              UNIT SELECT                                     PRM00291
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0292 P007C 0001          NUM   $1          RTZS                                    PRM00292
0293 P007D 0003          NUM   $3          MEMORY BANK SELECT                      PRM00293
0294 P007E 0007          NUM   $7          BLOCK LENGTH (NO. OF WORDS)             PRM00294
0295 P007F 0002          NUM   $2          FIRST WORD ADDRESS (FWA)                PRM00295
0296 P0080 000A          NUM   $A          SEEK (FOR READ/WRITE/WRITE TAGS/COMPARE) PRM00296
0297 P0081 0001        NUM  $1            READ/WRITE/WRITE ADDRESS TAGS           PRM00297
0298 P0082 0001        NUM  $1            COMPARE                                 PRM00298
0299 P0083 0006          NUM   $6          UNIT DESELECT                           PRM00299
0300 P0084 0008          NUM   $8          BUS RELEASE                             PRM00300

0302 P0085 0000  WATMSK  BSS   WATMSK(0)   MASK FOR WAITING ON STATUS              PRM00302
0303 P0085 0000          NUM   0           NO WAITTING AFTER CLEAR CONTROLLER      PRM00303
0304 P0086 0102          NUM   $0102       BUS CON.- WAIT FOR EOP                  PRM00304
0305 P0087 0102          NUM   $0102       UNIT SEL.- EOP                          PRM00305
0306 P0088 0010          NUM   $0010       RTZS-WAIT FOR "ON CYLINDER" (CONTROLLER PRM00306
0307                     *                 DOES NOT BECOME BUSY FOR RTZS).         PRM00307
0308 P0089 0000          NUM   0           BANK SELECT - DUMMY ENTRY (NOT USED)    PRM00308
0309 P008A 0000          NUM   0           BLOCK LENGTH - DUMMY ENTRY              PRM00309
0310 P008B 0000          NUM   0           FWA - DUMMY ENTRY                       PRM00310
0311 P008C 0112          NUM   $0112       SEEK - EOP % "ON CYLINDER"              PRM00311
0312 P008D 0102        NUM  $0102         READ/WRITE/WRITE ADDRESS TAGS - EOP     PRM00312
0313 P008E 0102        NUM  $0102         COMPARE - EOP                           PRM00313
0314 P008F 0102          NUM   $0102       UNIT DESELECT - EOP                     PRM00314
0315 P0090 0102          NUM   $0102       BUS RELEASE - EOP                       PRM00315

0317 P0091 0000  WATRSL  BSS   WATRSL(0)   RESULT OF STATUS "ANDED" WITH WATMSK IF PRM00317
0318                     *                 THE SPECIFIED EVENTS OCCURED (I.E.:THE  PRM00318
0319                     *                 PROGRAM SHOULD EXIT FROM WAITING LOOP). PRM00319
0320 P0091 0000          NUM   0           CLEAR CONTROLLER , COUNTINUE            PRM00320
0321 P0092 0100          NUM   $0100       EOP OF BUS CONNECT                      PRM00321
0322 P0093 0100          NUM   $0100       EOP OF UNIT SELECT                      PRM00322
0323 P0094 0010          NUM   $0010       "ON CYLINDER" FOR RTZS (ZERO SEEK)      PRM00323
0324 P0095 0000          NUM   0           BANK SELECT - DUMMY (NOT USED)          PRM00324
0325 P0096 0000          NUM   0           BLOCK LENGTH - DUMMY                    PRM00325
0326 P0097 0000          NUM   0           FWA - DUMMY                             PRM00326
0327 P0098 0110          NUM   $0110       EOP % "ON CYLINDER" FOR SEEK            PRM00327
0328 P0099 0100        NUM  $0100         EOP FOR READ/WRITE/WRITE ADDRESS TAGS   PRM00328
0329 P009A 0100        NUM  $0100         EOP FOR COMPARE                         PRM00329
0330 P009B 0100          NUM   $0100       EOP FOR UNIT DESELECT                   PRM00330
0331 P009C 0100          NUM   $0100       EOP FOR BUS RELEASE                     PRM00331

0333 P009D 0000  ERRMSK  BSS   ERRMSK(0)   MASK FOR CHECKING FOR ERRORS            PRM00333
0334 P009D 010E          NUM   $010E       CLEAR CONTROLLER                        PRM00334
0335 P009E 110A          NUM   $110A       BUS CONNECT                             PRM00335
0336 P009F 110A          NUM   $110A       UNIT SELECT                             PRM00336
0337 P00A0 311B          NUM   $311B       RTZS(% "ON CYLINDER")                   PRM00337
0338 P00A1 0000          NUM   0           BANK SELECT - DUMMY (NOT USED)          PRM00338
0339 P00A2 0000          NUM   0           BLOCK LENGTH - DUMMY                    PRM00339
0340 P00A3 0000          NUM   0           FWA - DUMMY                             PRM00340
0341 P00A4 311B          NUM   $311B       SEEK (% "ON CYLINDER")                  PRM00341
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0342 P00A5 311B          NUM  $311B        READ/WRITE/WRITE ADDRESS TAGS                    PRM00342
0343 P00A6 311B          NUM  $311B        COMPARE                                          PRM00343
0344 P00A7 110A          NUM  $110A          UNIT DESELECT                                  PRM00344
0345 P00A8 110A          NUM  $110A          BUS RELEASE                                    PRM00345

0347 P00A9 0000  ERRSLT  BSS  ERRSLT(0)      RESULT OF STATUS "ANDED" WITH ERRMSK IF          PRM00347
0348             *                           NO ERROR OCCURRED                              PRM00348
0349 P00A9 0100          NUM  $0100          CLEAR CONTROLLER - EOP                         PRM00349
0350 P00AA 1100          NUM  $1100          BUS CONNECT- "ON BUS" % EOP                    PRM00350
0351 P00AB 1100          NUM  $1100          UNIT SELECT - "ON BUS" % EOP                   PRM00351
0352 P00AC 1111          NUM  $1111          RTZS - "ON BUS % CYLINDER",READY % EOP         PRM00352
0353 P00AD 0000          NUM  0              BANK SELECT - DUMMY (NOT USED)                 PRM00353
0354 P00AE 0000          NUM  0              BLOCK LENGTH - DUMMY                           PRM00354
0355 P00AF 0000          NUM  0              FWA - DUMMY                                    PRM00355
0356 P00B0 1111          NUM  $1111          SEEK - "ON BUS % CYLINDER",READY % EOP         PRM00356
0357 P00B1 1111          NUM  $1111        READ/WRITE/TAGS: ON BUS,CYLINDER,READY, EOP      PRM00357
0358 P00B2 1111          NUM  $1111        COMPARE        : ON BUS,CYLINDER,READY, EOP      PRM00358
0359 P00B3 1100          NUM  $1100          UNIT DESELECT - "ON BUS" % EOP.                PRM00359
0360 P00B4 0100          NUM  $0100          BUS RELEASE - EOP.                             PRM00360

0362       00B5 P NEXTBL EQU      NEXTBL(*)  POINTER FOR ROUTINE TO BE EXECUTED AFTER:      PRM00362
0363 P00B5 002C          ADC*   NXINCI  I=0      CLEAR CONTROLLER                          PRM00363
0364 P00B6 002B          ADC*   NXINCI  I=1      BUS CONNECT                               PRM00364
0365 P00B7 0051          ADC*   NXUFIN  I=2      UNIT SELECT                               PRM00365
0366 P00B8 0029          ADC*   NXINCI  I=3      RTZS                                      PRM00366
0367 P00B9 0076          ADC*   NXBLKL  I=4      MEMORY BANK SELECT                        PRM00367
0368 P00BA 0027          ADC*   NXINCI  I=5      BLOCK LENGTH                              PRM00368
0369 P00BB 0026          ADC*   NXINCI  I=6      FIRST WORD ADDRESS                        PRM00369
0370 P00BC 006B          ADC*   NXRWPR  I=7      SEEK                                      PRM00370
0371 P00BD 006F          ADC*   NXRWCM  I=8      READ/WRITE/WRITE ADDRESS TAGS             PRM00371
0372 P00BE 0023          ADC*   NXINCI  I=9      COMPARE                                   PRM00372
0373 P00BF 0022          ADC*   NXINCI  I=10     UNIT DESELECT                             PRM00373
0374 P00C0 0072          ADC*   ENDREQ  I=11     BUS RELEASE                               PRM00374
0375             *                                                                          PRM00375
0376             *         END OF  OUTPUT OPERATIONS TABLE.                                 PRM00376
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0378                *       THE FOLLOWING IS THE LIST OF ALL EQU'S,NUM'S,AND BSS'S          PRM00378
0379                *       FOR THE PROGRAM( IN ALPHABETIC ORDER).                         PRM00379
0380                *                                                                      PRM00380
0381        000B    CMCODE  EQU   CMCODE(11)     L.S.BITS FOR A-REG. IN COMPARE INSTRUCTION PRM00381
0382 P00C1  0000    CMPFLG  NUM       0      COMPARE FLAG                                   PRM00382
0383        000E    DEVICE EQU  DEVICE(14)    EQUIPMENT NUMBER                             PRM00383
0384 P00C2  0701    EMASS   ADC       DEVICE*128+1  W.E.S.  FUNCTION CODE                 PRM00384
0385        0010    QSTTS   EQU   QSTTS($10)     Q REG. VALUE TO INPUT STATUS             PRM00385
0386        0009    RDCODE  EQU   RDCODE(9)      L.S.BITS FOR A-REG. IN READ INSTRUCTION  PRM00386
0387        0060    SCWRD   EQU   SCWRD(96)      NO.OF WORDS PER SECTOR                   PRM00387
0388        2010    SKERR   EQU   SKERR($2010)   MASK FOR SEEK ERROR & "ON CYLINDER" BITS PRM00388
0389        0010    SKRSL   EQU   SKRSL($10)     EXPECTED RESULT AFTER APPLYING SKERR     PRM00389
0390                *                            TO STATUS, IF NO ERROR                   PRM00390
0391                *                            SELECT WORDS.                            PRM00391
0392        0080    UNTSEL  EQU   UNTSEL($80)    UNIT 0 SELECT - A REG.                   PRM00392
0393        000D    WADCOD  EQU       WADCOD(13) L.S.BITS FOR A-REG. IN WRITE TAGS INSTR. PRM00393
0394        000A    WRCODE  EQU   WRCODE(10)     L.S.BITS FOR A-REG. IN WRITE INSTRUCTION PRM00394
0395        0020    WRPRTC  EQU       WRPRTC($20)  MASK FOR WRITE PROTECTED               PRM00395
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0397                *       Q M A S S -  I N I T I A L I Z E R                          PRM00397
0398                *                                                                   PRM00398
0399                *       THE FOLLOWING ROUTINE SAVES THE INPUT PARAMETERS AND CHECKS  PRM00399
0400                *       WHETHER THE REQUEST IS FOR READ OR  WRITE OPERATIONS.       PRM00400
0401                *                                                                   PRM00401
0402 P00C3 0000     QMASS   NUM  0                                                      PRM00402
0403 P00C4 0844             CLR  A                                                      PRM00403
0404 P00C5 6842             STA* IOINDX      SET IOINDX TO BEGIN OF OUTPUT TABLE        PRM00404
0405 P00C6 181C             JMP* DOUT                                                   PRM00405

0407                *       E R R O R        R O U T I N E                              PRM00407

0409                *       IN ENTRY LOCATION 'DYNST' CONTAIN LAST HARDWARE STATUS       PRM00409
0410                *       ENTRIES  EROUT IS FOR EXTERNAL/INTERNAL REJECT  REG.Q = 6/5  PRM00410
0411                *                ERROR2 IS FOR ILLEGAL REQUESTA         REG.Q = 74   PRM00411
0412                *                ERROR3 IS FOR NOT READY ERROR          REG.Q = 14   PRM00412
0413                *                ERROR  IS FOR DYNAMIC STATUS ERROR                  PRM00413
0414                *                       IF DEVICE SEEK ERROR IS ON      REG.Q = 17   PRM00414
0415                *                          ELSE IF BUS IS OFF           REG.Q = 70   PRM00415
0416                *                             ELSE IF ALARM BIT IS ON                 PRM00416
0417                *                             AND COMPARE FLAG IS ON       REG.Q = 7  PRM00417
0418                *                                ELSE IT IS ALARM ERROR    REG.Q = 2  PRM00418
0419                *                       IF GHOST ERROR HAPPENED          REG.Q = FF  PRM00419

0421 P00C7 C86C     EROUT   LDA* DYNST                                                  PRM00421
0422 P00C8 18FF     DSKERR  NUM  $18FF       HANG IF DISK ERROR                         PRM00422
0423 P00C9 0C4A     ERROR2  ENQ      74      FOR SECTOR ADDRESS GREATER THEN POSSIBLE   PRM00423
0424 P00CA 18FC             JMP*     EROUT                  FOR THIS DEVICE             PRM00424
0425 P00CB 0C0E     ERROR3  ENQ      14      FOR NOT READY ERROR                        PRM00425
0426 P00CC 18FA             JMP*     EROUT                                              PRM00426
0427 P00CD E866     ERROR   LDQ* DYNST       CHECK DYNAMIC STATUS                       PRM00427
0428 P00CE 0FA2             QLS      2                                                  PRM00428
0429 P00CF 0162             SQP      ER1     SKIP IF NOT DEVICE SEEK ERROR              PRM00429
0430 P00D0 0C11             ENQ      17                                                 PRM00430
0431 P00D1 18F5             JMP*     EROUT                                              PRM00431
0432 P00D2 0FA1     ER1     QLS      1                                                  PRM00432
0433 P00D3 0172             SQM      ER2     SKIP IF BUS OFF                            PRM00433
0434 P00D4 0C46             ENQ      70                                                 PRM00434
0435 P00D5 18F1             JMP*     EROUT                                              PRM00435
0436 P00D6 0FA9     ER2     QLS      9                                                  PRM00436
0437 P00D7 0167             SQP      ER3     SKIP IF NOT ALARM ERROR                    PRM00437
0438 P00D8 C82F         LDA* IOINDX                                                    PRM00438
0439 P00D9 09F6         INA  AVEC-ACOMP      IF ALARM HAPPENED DURING COMPARE          PRM00439
0440 P00DA 0112             SAN      ER4             OPERATION THEN NO COMPARE ERROR    PRM00440
0441 P00DB 0C07             ENQ      7                                                  PRM00441
0442 P00DC 18EA             JMP*     EROUT                                              PRM00442
0443 P00DD 0C02     ER4     ENQ      2               ELSE ALARM ERROR                   PRM00443
0444 P00DE 18E8             JMP*     EROUT                                              PRM00444
0445 P00DF 0CFF     ER3     ENQ      -0      IF GHOST ERROR                             PRM00445
0446 P00E0 18E6         JMP* EROUT                                                     PRM00446
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0448                *       O U T P U T   C Y C L E   -   M A I N   P R O G R A M                PRM00448
0449                *                                                                            PRM00449
0450                *       THE FOLLOWING ROUTINE IS THE MAIN PROGRAM. IT EXECUTES ALL           PRM00450
0451                *       OUTPUT OPERATIONS,ACCORDING TO THEIR ORDER IN THE TABLE.             PRM00451
0452                *       IT INCREMENTS I BY 1 TO POINT TO THE NEXT I/O,JUMPS TO               PRM00452
0453                *       PRE-OUTPUT ROUTINE,EXECUTES OUTPUT,WAITS ON STATUS & CHECKS          PRM00453
0454                *       FOR ERRORS AND JUMPS TO A POST-OUTPUT ROUTINE.                       PRM00454
0455                *        PRE & POST OUTPUT ROUTINES ENABLE THE PROGRAMMER TO SET             PRM00455
0456                *        PARAMETERS,CHECK CONDITIONS AND CHANGE THE PROGRAM FLOW .           PRM00456
0457                *        A RETURN TO DOUT WILL CAUSE THE OUTPUT (POINTED TO BY I REG)        PRM00457
0458                *        TO BE EXECUTED.A RETURN TO PMPOST CAUSES A SKIP ON THE              PRM00458
0459                *        OUTPUT OPERATION.A RETURN TO INCRI CAUSES THE NEXT                  PRM00459
0460                *        OUTPUT TO BE EXECUTED.                                              PRM00460
0461                *       NOTICE THAT AN OUTPUT MAY BE REPEATED SIMPLY BY COMING BACK          PRM00461
0462                *       TO THE INSTRUCTION FOLLOWING  THE ; RAO- I .                         PRM00462
0463                *       ON RETURNING TO THIS  ROUTINE - I MUST BE RESTORED.                  PRM00463
0464                *                                                                            PRM00464
0465 P00E1 D826    NXINCI RAO* IOINDX          MOVE TO NEXT OUTPUT                              PRM00465
0466 P00E2 5807    DOUT   RTJ*     OUTPUT      EXECUTE OUTPUT OPERATION                         PRM00466
0467 P00E3 5814    DOSTTS RTJ*     STTS        WAIT ACCORDING WA,SK & CHECK IF ERRORS           PRM00467
0468 P00E4 18E8    ERR    JMP*     ERROR       ERROR EXIT                                       PRM00468
0469 P00E5 E822    GONXT  LDQ* IOINDX          CONTINUE                                         PRM00469
0470 P00E6 FACE           ADQ* NEXTBL,Q        NEXT                                             PRM00470
0471 P00E7 1ACD           JMP* NEXTBL,Q        OPERATION                                        PRM00471
0472 P00E8 1BCC           JMP*     NEXTBL,B    CONTINUE NEXT OPERATION                          PRM00472

0474                *       O U T P U T                                                          PRM00474
0475                *                                                                            PRM00475
0476                *       THE FOLLOWING ROUTINE EXECUTES ALL OUTPUT OPERATIONS.                PRM00476
0477                *       ON ENTRY, I POINTS TO THE REQUIRED OUTPUT IN THE OUTPUT              PRM00477
0478                *       TABLE.                                                               PRM00478
0479                *                                                                            PRM00479
0480 P00E9 0000    OUTPUT NUM   0                                                               PRM00480
0481 P00EA E81D           LDQ* IOINDX                                                          PRM00481
0482 P00EB CA00           LDA  AVEC,Q          GET A-REG                                       PRM00482
     P00EC FF80
0483 P00ED EA8B           LDQ* QVEC,Q          GET Q-REG                                       PRM00483
0484 P00EE F8D3             ADQ*     EMASS      ADD EQUIPMENT CODE                              PRM00484
0485 P00EF 0DFE             INQ      -1                                                         PRM00485
0486 P00F0 0302           OUT   REJCT-*         EXECUTE OUTPUT                                  PRM00486
0487 P00F1 1CF7    PP3    JMP*  (OUTPUT)        RETURN                                          PRM00487
0488 P00F2 1803    REJCT    JMP*     INTREJ     FOR INTERNAL REJECT                             PRM00488
0489 P00F3 0C06             ENQ      6          ENTER  Q EXTERNAL  REJECT CODE                  PRM00489
0490 P00F4 1802             JMP*     OUTRJC     EXIT TO ERROR ROUTINE                           PRM00490
0491 P00F5 0C05    INTREJ   ENQ      5          ENTER Q INTERNAL REJECT CODE                    PRM00491
0492 P00F6 18D0    OUTRJC   JMP*     EROUT      EXIT TO ERROR ROUTINE                           PRM00492
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0494                *       S T A T U S                                                 PRM00494
0495                *       THE FOLLOWING ROUTINE READS THE DYNAMIC STATUS,WAITS UNTIL   PRM00495
0496                *       SPECIFIED EVENTS OCCUR, AND THEN CHECKS IF THERE WERE ANY    PRM00496
0497                *       SPECIFIED ERRORS.IF THERE WERE ERRORS IT RETURNS TO THE NEXT PRM00497
0498                *       INSTRUCTION IN THE CALLING PROGRAM. IF NO ERROR-IT SKIPS ON  PRM00498
0499                *       IT ( ASSUMING THAT IT IS A ONE-WORD INSTRUCTION).            PRM00499
0500                *       ON ENTRY, I POINTS TO THE CURRENT OUTPUT OPERATION           PRM00500
0501                *                                                                   PRM00501
0502 P00F7 0000    STTS    NUM   0                                                     PRM00502
0503 P00F8 0C0F    PS2     ENQ   QSTTS-1         SET Q REG FOR STATUS READING          PRM00503
0504 P00F9 F8C8             ADQ*      EMASS      ADD EQUIPMENT CODE                    PRM00504
0505 P00FA 02F7             INP       REJCT-*    TAKE STATUS , NO EXTERNAL REJECT      PRM00505
0506 P00FB 6838           STA* DYNST             SAVE STATUS                           PRM00506
0507 P00FC E80B           LDQ* IOINDX                                                  PRM00507
0508 P00FD AA87           AND* WAITMSK,Q         EXTRACT BITS TO WAIT ON               PRM00508
0509 P00FE BA92           EOR* WAITRSL,Q         CHECK WITH EXPECTED RESULT            PRM00509
0510 P00FF 0101            SAZ   PS1               DO ALL BITS MATCH ?                 PRM00510
0511 P0100 18F7            JMP*  PS2               READ ANOTHER STATUS AND CHECK AGAIN PRM00511
0512 P0101 C832    PS1     LDA* DYNST             GET STATUS                            PRM00512
0513 P0102 AA9A           AND* ERRMSK,Q          EXTRACT BITS THAT INDICATE POSSIBLE ERRORS PRM00513
0514 P0103 BAA5           EOR* ERRSLT,Q          CHECK WITH BIT SETTING FOR NO ERROR   PRM00514
0515 P0104 0111            SAN   PS3               IS THERE AN ERROR ?                 PRM00515
0516 P0105 D8F1            RAO*  STTS              NO, SKIP ONE INSTRUCTION ON RETURN  PRM00516
0517 P0106 1CF0    PS3     JMP*  (STTS)            RETURN                              PRM00517
0518                *                                                                   PRM00518
0519                *                                                                   PRM00519
0520 P0107 0000    IOINDX NUM  0                                                       PRM00520
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0522 P0108 E82B   NXUFIN LDQ* DYNST          RETURN AFTER UNIT SELECT                                  PRM00522
0523 P0109 0F61          LRS     1           SHIFT "READY" BIT INTO A                                  PRM00523
0524 P010A 013E          SAM     U1          IF READY SET UNIT DE-SELECT AND COUNTINUE                 PRM00524
     P010B C800          LDA  PWFFLG                                                                   PRM00525
     P010C FF5D
0526 P010D 011A          SAN  U2             SKIP IF NOT POWER FAILURE                                 PRM00526
0527                     LFA  AUNTSL,5,2                                                               PRM00527
0527 P010E 0584
0527 P010F 5100
0527 P0110 FF5E
0528 P0111 09FC          INA  -3             IF ALL UNITS TESTED                                       PRM00528
0529 P0112 0105          SAZ  U2             GO TO U2                                                  PRM00529
0530 P0113 0904          INA  4              ELSE CONNECT NEXT UNIT                                    PRM00530
0531                     SFA  AUNTSL,5,2                                                               PRM00531
0531 P0114 0585
0531 P0115 5100
0531 P0116 FF58
0532 P0117 18CA          JMP* DOUT                                                                     PRM00532
0533              *                                                                                    PRM00533
0534 P0118 18B2   U2       JMP*     ERROR3 EXIT TO ERROR ROUTINE                                      PRM00534
0535 P0119 C800   U1       LDA      AUNTSL GET THE SELECTED UNIT                                      PRM00535
     P011A FF54
0536 P011B B000            EOR      =XUNTSEL                                                          PRM00536
     P011C 0080
0537 P011D 6800            STA      AUNTDS STORE IN AVEC FOR UNIT DE-SELECT OPERATION                 PRM00537
     P011E FF58

0539              *        P R E   R T Z S   % W R I T E   T A G S                                      PRM00539
0540              *                                                                                    PRM00540
0541              *        CHECK IF SEEK ERROR BIT IS SET,OR IF "ON CYLINDER" BIT                      PRM00541
0542              *        IS RESET.IF SO,EXECUTE  RETURN TO ZERO SEEK (RTZS ) TO RESET                PRM00542
0543              *        ANY SEEK ERROR AND TO RECALIBRATE THE SELECTED UNIT.                        PRM00543
0544              *        OTHERWISE - SKIP ON RTZS.                                                   PRM00544
0545              *                                                                                    PRM00545
0546 P011F C814          LDA* DYNST          GET STATUS                                                PRM00546
0547 P0120 A000            AND    =XSKERR        MASK SEEK ERROR % "ON CYLINDER"BITS                   PRM00547
     P0121 2010
0548 P0122 B000            EOR    =XSKRSL        CHECK IF ERROR OR NOT ON CYLINDER                     PRM00548
     P0123 0010
0549 P0124 0111            SAN       RZ       SKIP, IF ERROR TO EXECUTE RTZS                         PRM00549

0551 P0125 D8E1          RAO* IOINDX                                                                   PRM00551
0552 P0126 18BA   RZ       JMP*     NXINCI      RETURN  TO MAIN ROUTINE                                PRM00552
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0555                *       P R E   R E A D / W R I T E / C O M P A R E / T A G S          PRM00555
0556 P0127 C899     NXRWPR  LDA* CMPFLG                                                    PRM00556
0557 P0128 D898             RAO* CMPFLG                                                    PRM00557
0558 P0129 0101             SAZ  1          SKIP IF READ/WRITE OR TAGS STILL TO BE DONE    PRM00558
0559 P012A D8DC     P9      RAO* IOINDX     ELSE INCREASE IOINDX AND EXECUTE COMPARE       PRM00559
0560 P012B 18B5             JMP* NXINCI                                                    PRM00560
0561                *                                                                      PRM00561
0562                *       P O S T   R E A D / W R I T E / C O M P A R E / T A G S        PRM00562
0563                *                                                                      PRM00563
0564 P012C 0A04     NXRWCM  ENA  ABNKSL-AVEC  DO COMPARE                                    PRM00564
0565 P012D 68D9             STA* IOINDX                                                    PRM00565
0566 P012E 18B2             JMP* NXINCI                                                    PRM00566
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0568                    *       P R E   B L O C K   L E N G T H                 PRM00568
0569                    *                                                       PRM00569
0570                    *       THE FOLLOWING CALCULATES THE DISK CYLINDER,SURFACE AND  PRM00570
0571                    *       SECTOR FROM THE ADDRESS OF THE STARTING SECTOR. PRM00571
0572                    *                                                       PRM00572
0573          012F P NXBLKL EQU  NXBLKL(*)                                      PRM00573
0574 P012F 0844         CLR  A                                                  PRM00574
0575 P0130 6890         STA* CMPFLG                                             PRM00575
0576 P0131 18AF         JMP* NXINCI                                             PRM00576


0578                    *                                                       PRM00578
0579                    *       E N D   R E Q U E S T                           PRM00579
0580                    *                                                       PRM00580
0581                    *       FINISH THE REQUEST :                            PRM00581
0582                    *                                                       PRM00582
0583 P0132 0000 ENDREQ  BSS  ENDREQ(0)      NO-ERROR ENTRY                      PRM00583
0584 P0132 1C90         JMP* (QMASS)        RETURN TO CALLING ROUTINE           PRM00584
0585 P0133 0000 DYNST   NUM  0              DYNAMIC STATUS                      PRM00585
0586                    *                                                       PRM00586
0587 P0134 A85A CHKSUM  NUM  $A85A                                              PRM00587
0588          0134 P PROMND EQU  PROMND(*-1)                                    PRM00588
0589          0104   PROML  EQU  PROML(*-PROM)                                  PRM00589


0591                    *                                                       PRM00591
0592                    PCC  K0C00;         SET P = $0C00                       PRM00592
0592 P0135 4B30
     P0136 4330
     P0137 303A
0593                    PCC  I:             START EXECUTION                     PRM00593
0593 P0138 493A
0594                    PCC  J40@           ENABLE CONSOLE TRANSMIT             PRM00594
0594 P0139 4A34
     P013A 3040
0595 P013B BB00         NUM  $BB00          TERMINATE LOADING                   PRM00595


0597                    END  0                                                  PRM00597
```

PGM= 013C (316) COM = 0000 (0) DAT = 0000 (0)

*** S Y M B O L T A B L E ***

ABNKSL	0071P	ABSCON	006EP	ABSREL	0078P	ACLCNT	006DP	ACOM[illegible]	0076P
AFWA	0073P	ALNGTH	0072P	ARDWRC	0075P	ARTZS	0070P	ASKR[illegible]	0074P
AUNTDS	0077P	AUNTSL	006FP	AVEC	006DP	CHKSUM	0134P	CKSE[illegible]	0036P
CLEAR	003CP	CLRLP1	0041P	CLRLP2	0045P	CMCODE	000B	CMPF[illegible]	00C1P
DELLP	0056P	DENSTY	0002	DEVICE	000E	DOSTTS	00E3P	DOUT	00E2P
DSKERR	00C8P	DYNST	0133P	EMASS	00C2P	ENDREQ	0132P	ER1	00D2P
ER2	00D6P	ER3	00DFP	ER4	00DDP	EROUT	00C7P	ERR	00E4P
ERRMSK	009DP	ERROR	00CDP	ERROR2	00C9P	ERROR3	00CBP	ERRS[illegible]	00A9P
GONXT	00E5P	HERE	003AP	HFFFF	006CP	I	00FF	INTR[illegible]	00F5P
IOINDX	0107P	LPMSK	0002	MC	0000P	NEXTBL	0065P	NOTP[illegible]	005CP
NSEC	0078	NXBLKL	012FP	NXINCI	00E1P	NXRWCM	012CP	NXRW[illegible]	0127P
NXUFIN	0108P	OK	0039P	OUTPUT	00E9P	OUTRJC	00F6P	P1	0003P
P2	0005P	P2S	0020P	P3S	0030P	P9	012AP	PAJU[illegible]	0060
PASPPS	0041	PP3	00F1P	PROM	0031P	PROML	0104	PS1	0101P
PS2	00F8P	PS3	0106P	PWFFLG	006AP	QMASS	00C3P	QSTT[illegible]	0010
QVEC	0079P	RDCODE	0009	RDDSK	0063P	REJCT	00F2P	RPMS[illegible]	0012
R2	0126P	SCWRD	0060	SETPB	004DP	SETPPS	0020P	SKER[illegible]	2010
SKRSL	0010	STTS	00F7P	U1	0119P	U2	0116P	UNTS[illegible]	0060
WADCOD	000D	WAJUMP	0030	WASPPS	0020	WATMSK	0085P	WATR[illegible]	0091P
WRCODE	000A	WRPRTC	0020	ZERO	006BP				

*** E X T / E N T T A B L E ***

PROMND 0134P PROMST 0031P